

# IH67D-MHT REV 6.0

## CPU:

Intel Sandy Bridge processors in LGA1155 Package 95W

## System Chipset:

Sugar Point

## Main Memory:

Dual Channel/DDR-III\*4(Max 16GB) 1066/1333  
DDR3-1333 /1066

## Onboard Device:

Super I/O:IT8728

LAN:Realtek 8111E

HD Codec:ALC892 3 jacks

PCI BRIDGE:IT8893E

## Power solution:

CPU Voltage Regulators:3phase by uP6235 high 1 low 2 OV BY UP6262 MOSFET HEARSINK

AXG voltage Regulators:1phase by uP6235 high 1 low 2

VTT voltage Regulators:1Phase by UP6109 high 1 low 2 OV BY UP6262 MOSFET HEARSINK

DDR voltage Regulators:1Phase by UP6109 high 1 low 1 OV BY UP6262

## Expansion Slots:

PCI EXPRESS 16X SLOT\*2

PCI EXPRESS 1X SLOT\*1

PCI SLOT\*1

## REAR IO:

PS/2 +2 layer USB2.0 Port

HDMI Port

DVI Port

VGA Port

2 layer USB2.0 + Gb RJ-45 Ports

Audio Jacks

## Front I/O:

4SATA2(Red)+ 2SATA3(white)

USB Header \* 3


CPU /System1/System2 FAN

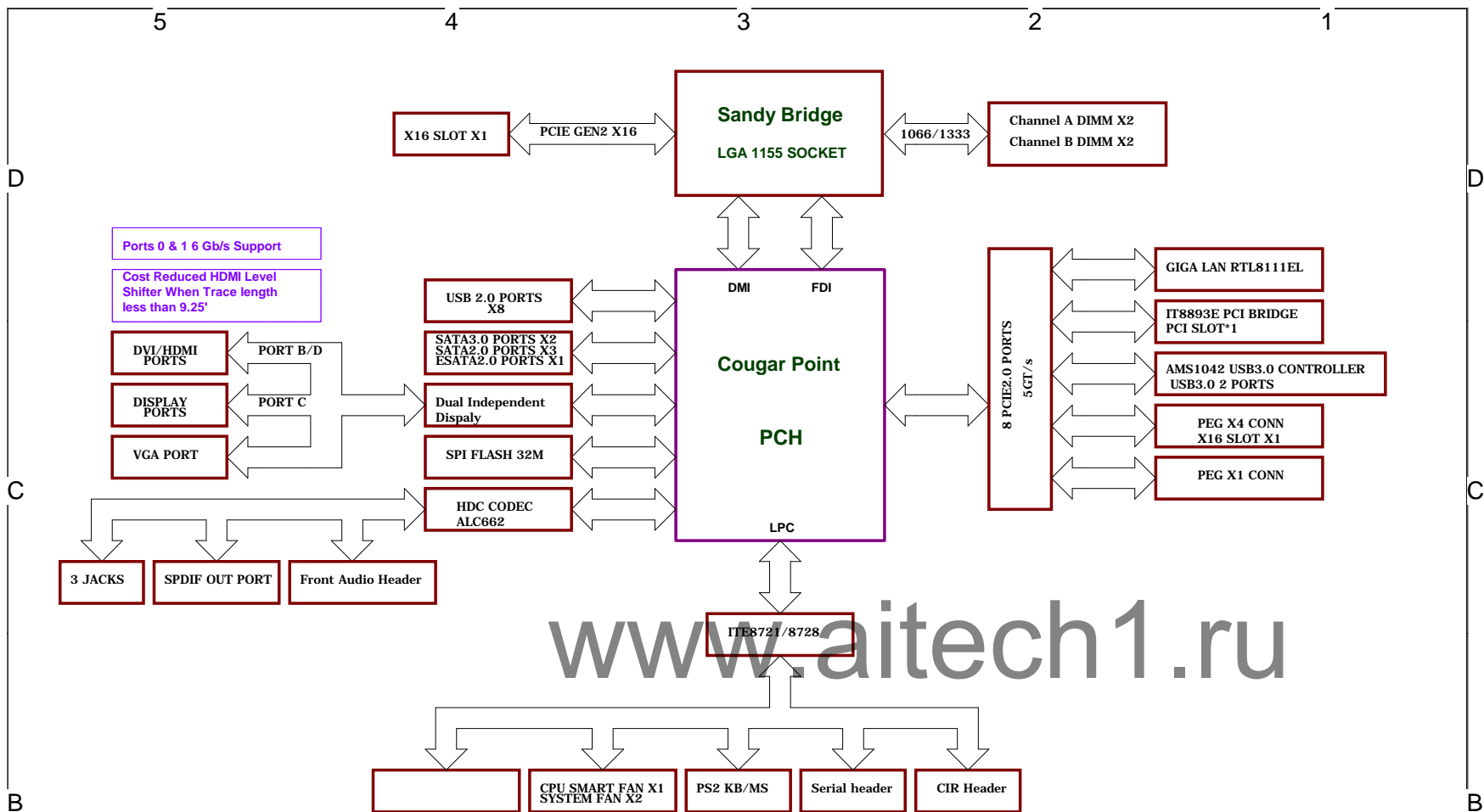
Serial header

CIR Header

Front Audio Header & SPDIF Out 1

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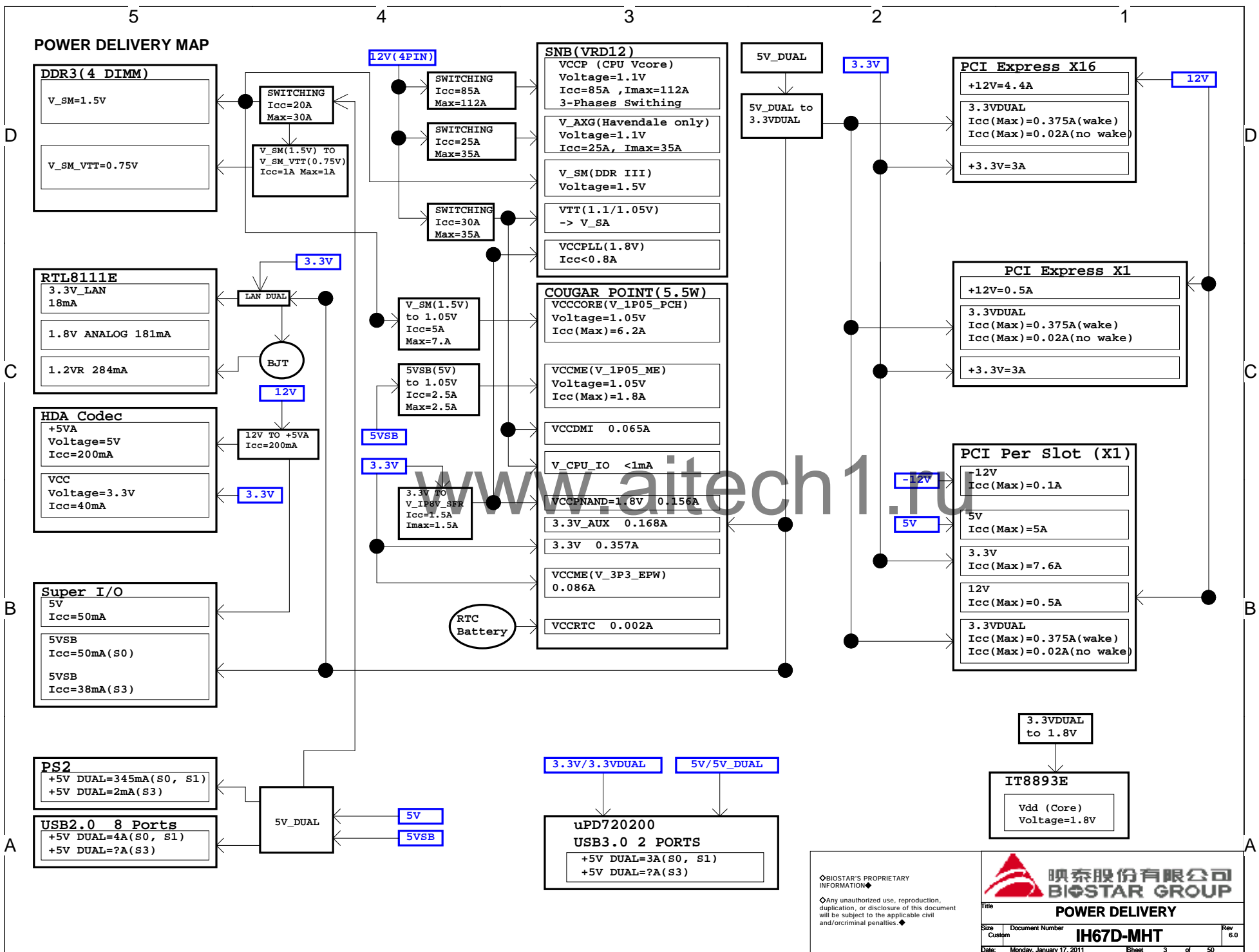


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Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
PCI Express* 2.0 Ports	8	8	8	8	8	6 <sup>9</sup>
PCI Interface	Yes	Yes	Yes	No <sup>10</sup>	No <sup>10</sup>	No <sup>10</sup>
USB 2.0 Ports	14	14	12 <sup>6</sup>	14	14	10 <sup>7</sup>
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 <sup>4</sup>	1 <sup>5</sup>	1 <sup>5</sup>	2 <sup>4</sup>	2 <sup>4</sup>	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4 <sup>8</sup>
HDMI/DVI/VGA/DisplayPort*/eDP*	Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP	Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	No
	RAID 0/1/5/10 Support	Yes	No	No	Yes	No
Intel® AT	Yes	Yes	No	No	No	No
Intel® AMT 7.0	Yes	No	No	No	No	No
Intel® Remote PC Assist Technology - Proactive	Yes	No	Yes	No	No	No
Intel® Remote PC Assist Technology - Reactive	No	No	Yes	Yes	No	No

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<b>BLOCK DIAGRAM</b>		
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## IH67B-MHT REV 0.6 TO 0.61 CHANGELIST

- 1.YR86,YR87 NI
- 2.YR84,YR85 NI
- 3.YR67,YR83 NI
4. ADD C30
- 5.ADD YR75; YR64&YR65 NI; Remove DP signal
- 6.YR73 NI
- 7.YR77&YR78 change from 100ohm to 10ohm; YC17 change from 0.1uf to 1uf
- 8.Add page 25 content
- 9.Page 26: all By16 signal AC couple cap change from 0.1uf to 0.22uf for PCIE3.0 compatible
- 10.ER7 reserved; EU1.5 connect to power; EU1.59 connect to power; Add ER18; ER8 NI,ER9 reserved; ER12 NI,ER13 reserved; ER16 NI; Add ERN9&ERN10
- 11.HDMI\_DP1 change to HDMI
- 12.Remove page 32 content(DP port)
- 13.Removed ARN3; add AR29, AR30, AR31, AR32; AR29& AR30 NI
- 14.Add SQ7,SQ8,SQ9,FAN\_TACH sch changed
- 15.Reserve Q18
- 16.NI R71,R74,R78,Q43,Q44
- 17.CT10 change from 820UF-S 2.5V 6.3X8 ELITE to 820UF-S 2.5V 6.3X8
- 18.TR24.1 connect to V\_SA
- 19.Page 47:change from UP6230 to UP6235; Add page48 content
- 20.Page50:V\_1P05\_ME power solution changed; ME power NI;
- 21.Page51:change from ASM1042 to uPD720200
- 22.Add VCCP\_SEL circuit
- 23.CR28 change from 0ohm to 120ohm
- 24.Remove YRN11,add YR76,YR89,YR90
- 25.Remove YR43,YR change from 1.1Kohm to 200ohm
- 26.Remove YC20,BYC21,YC28,BYC29,YC35,YC36
- 27.Remove EU2,ERN1
- 28.Add Q10
- 29.Add R24
- 30.Modify +3V3\_DUAL solution

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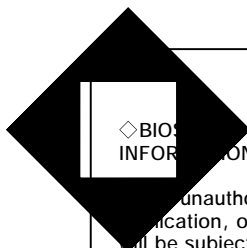
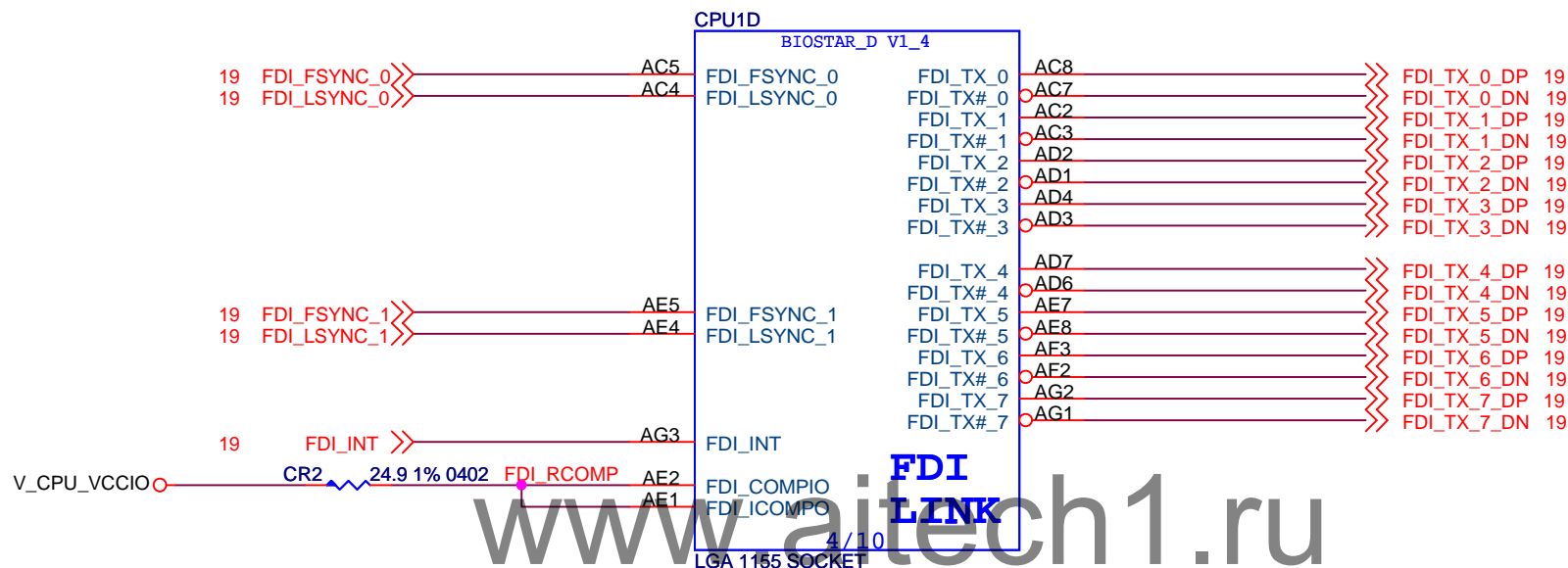


A



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# CPU PART: C+Reference



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DQ REMAPPING IMPLEMENTED  
TO IMPROVE BREAKOUT AND  
MINIMIZE CH-2-CH COUPLING

Q 40  
Q 41  
Q 42  
Q 43  
Q 44  
Q 45  
Q 46  
Q 47  
Q 48

SB CK#0  
SB CK#0  
SB CK#1  
SB CK#1  
SB CK#1  
SB CK#2

AL21  
AL22  
AL20  
AL20  
AL20  
AL23

2CK DDR0 B DP 13  
2CK DDR0 B DN 13  
2CK DDR1 B DP 13  
2CK DDR1 B DN 13  
2CK DDR2 B DP 13

DDR\_1

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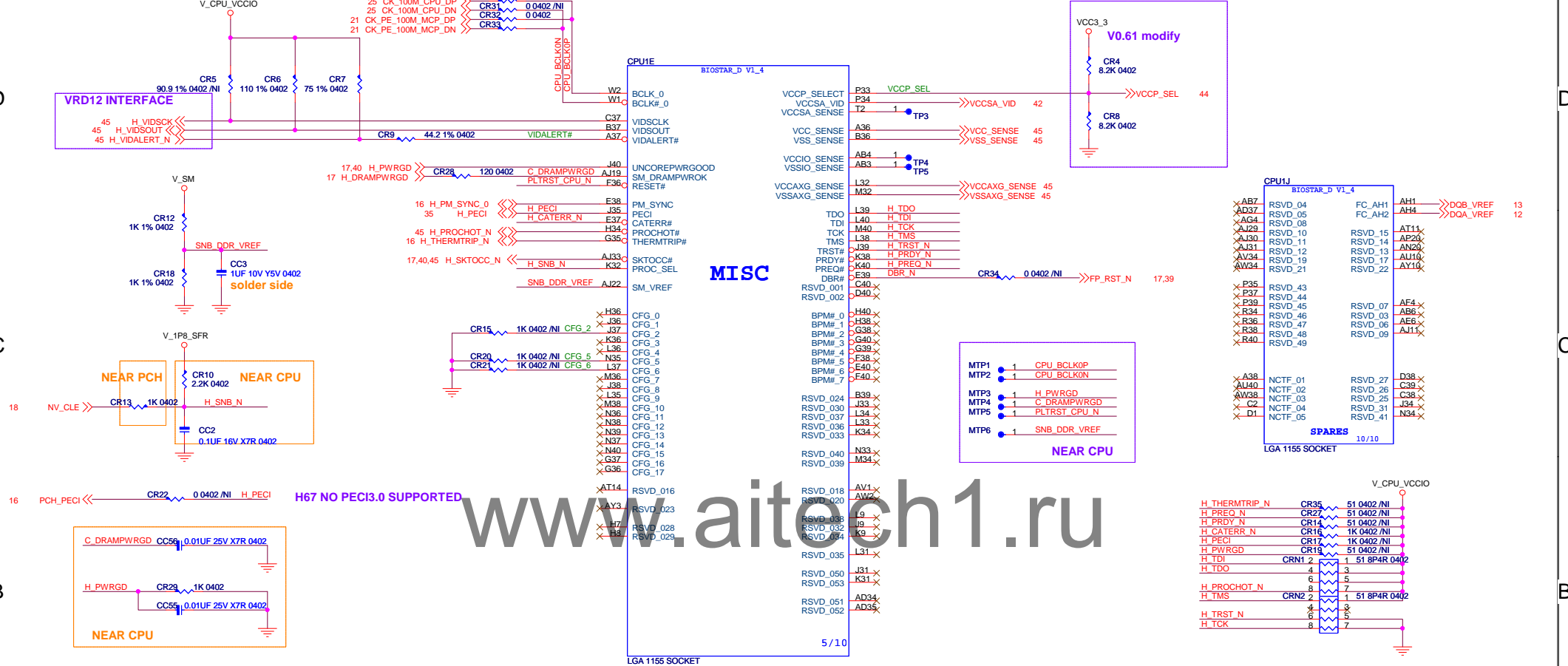
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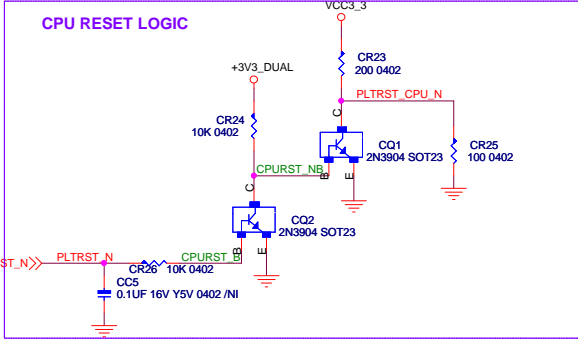
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# CPU PART: C+Reference



CFG6	CFG5	PCIE CONFIG
1	1	1 X 16
1	0	2 X 8
0	1	RESERVED
0	0	X8,X4,X4

CFG	H	L	DESCRIPTION
2	NORM	RESERVED	PEGLANE REVERSAL[0],X16
5	*	*	SEL0
6	*	*	SEL1



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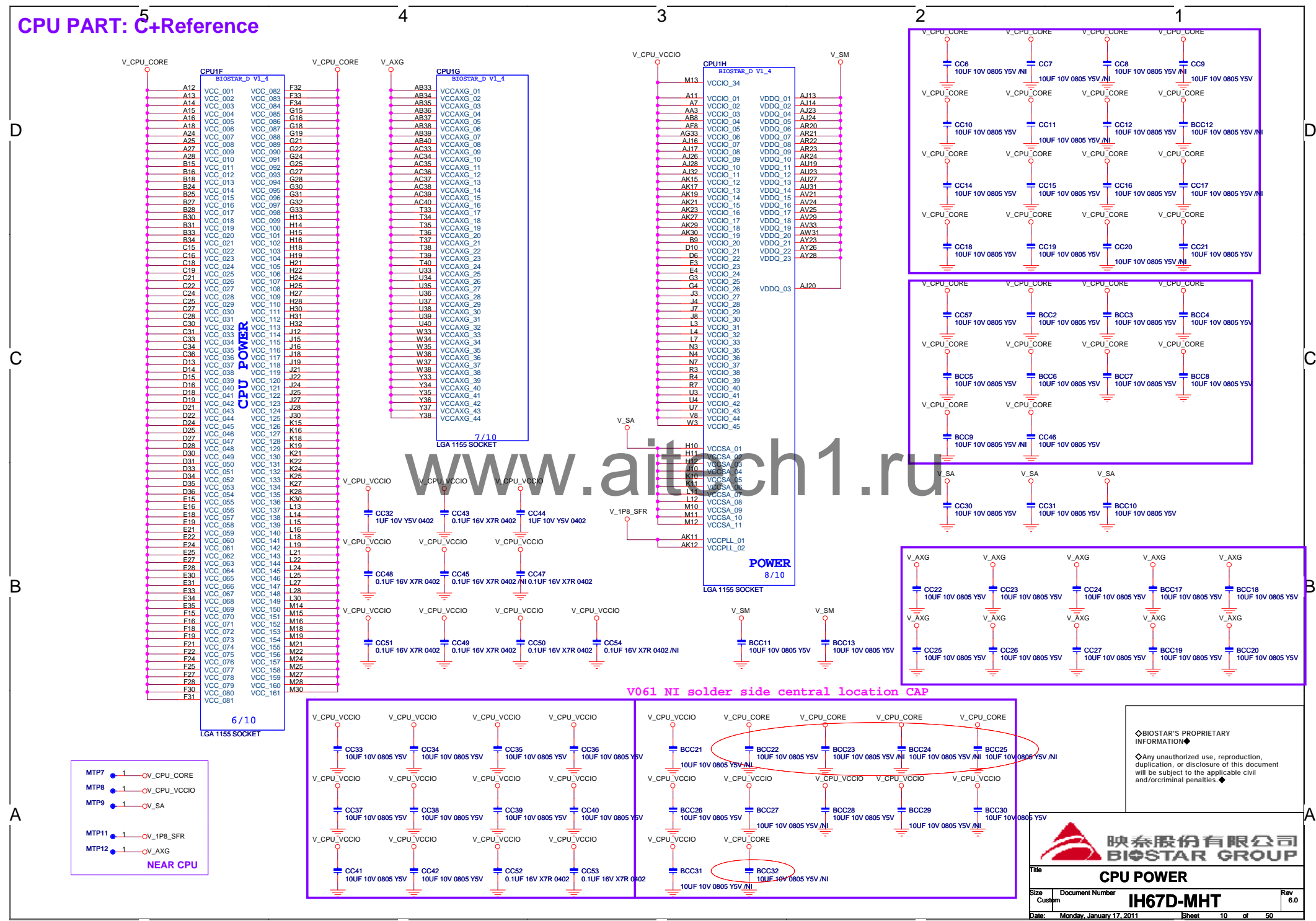
**CPU MISC**

**IH67D-MHT**

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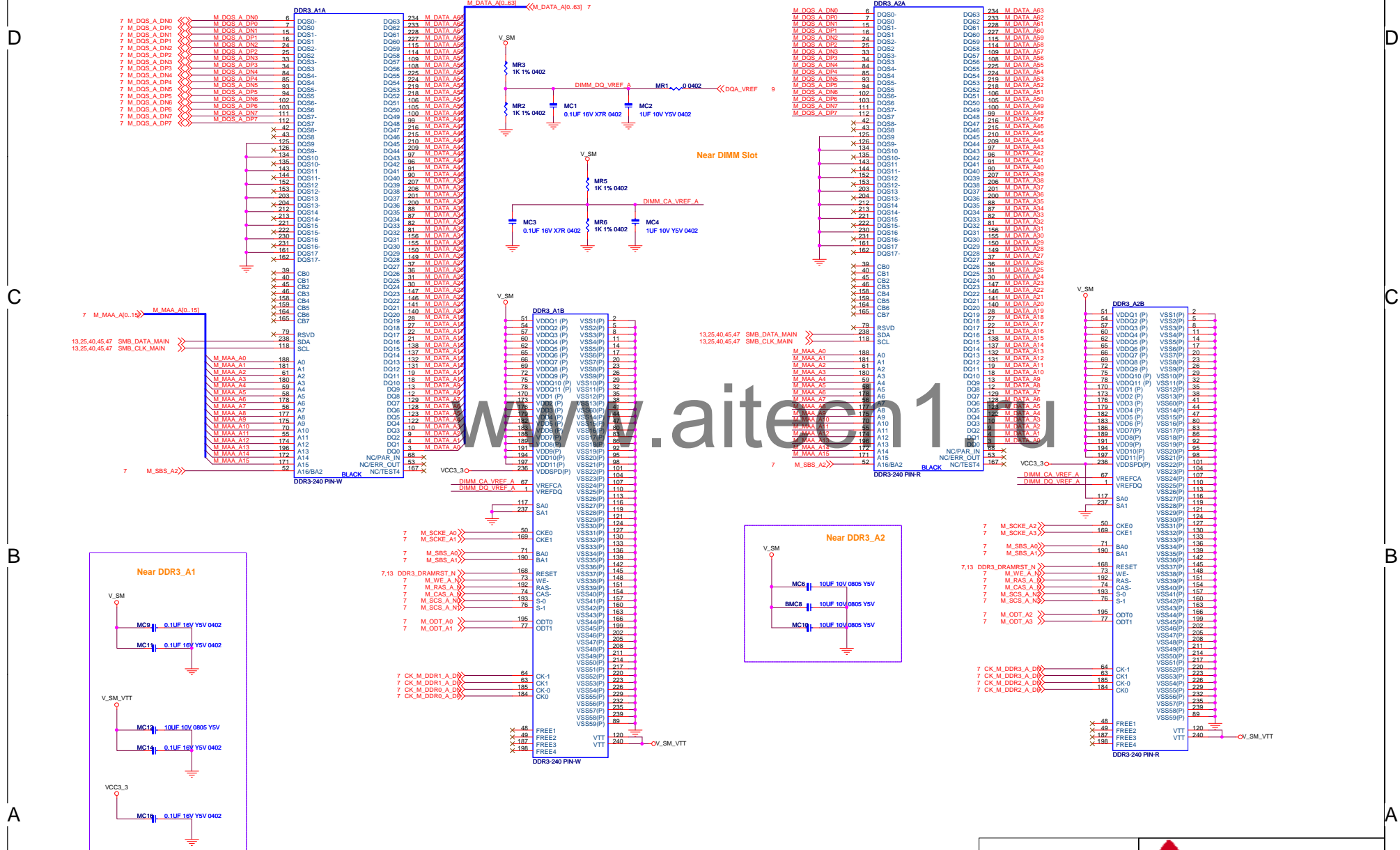
# CPU PART: C+Reference







## 5 MEMORY PART. M+Reference





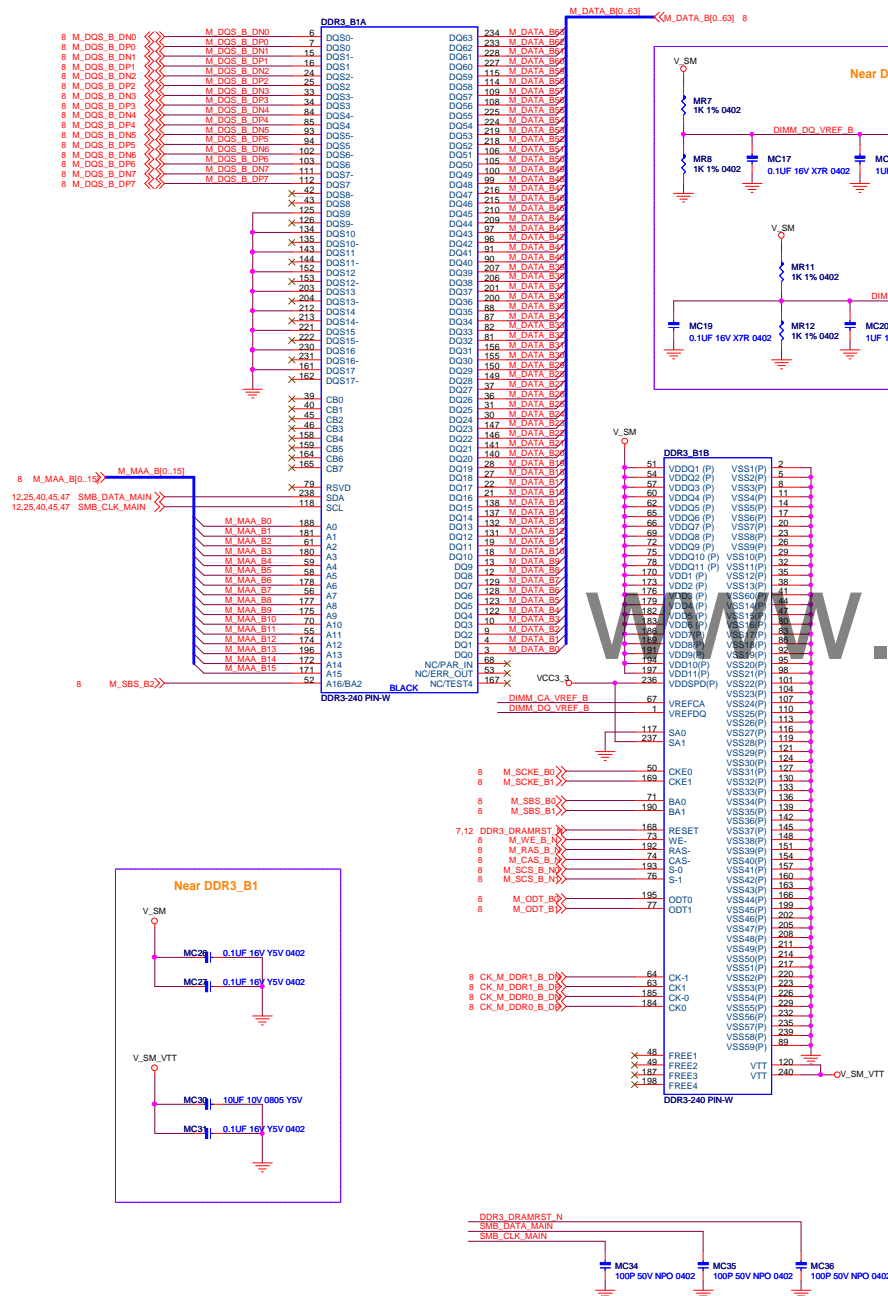
# MEMORY PART: M+Reference

D

C

B

A



# PCH PART: Y+Reference

**Internal Pull up**

**PCI**

**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
0	1	NANO
1	0	PCI
1	1	SPI

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**PCH PART: Y+Reference**

**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

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**PCH PART: Y+Reference**

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**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

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**PCH PART: Y+Reference**

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**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

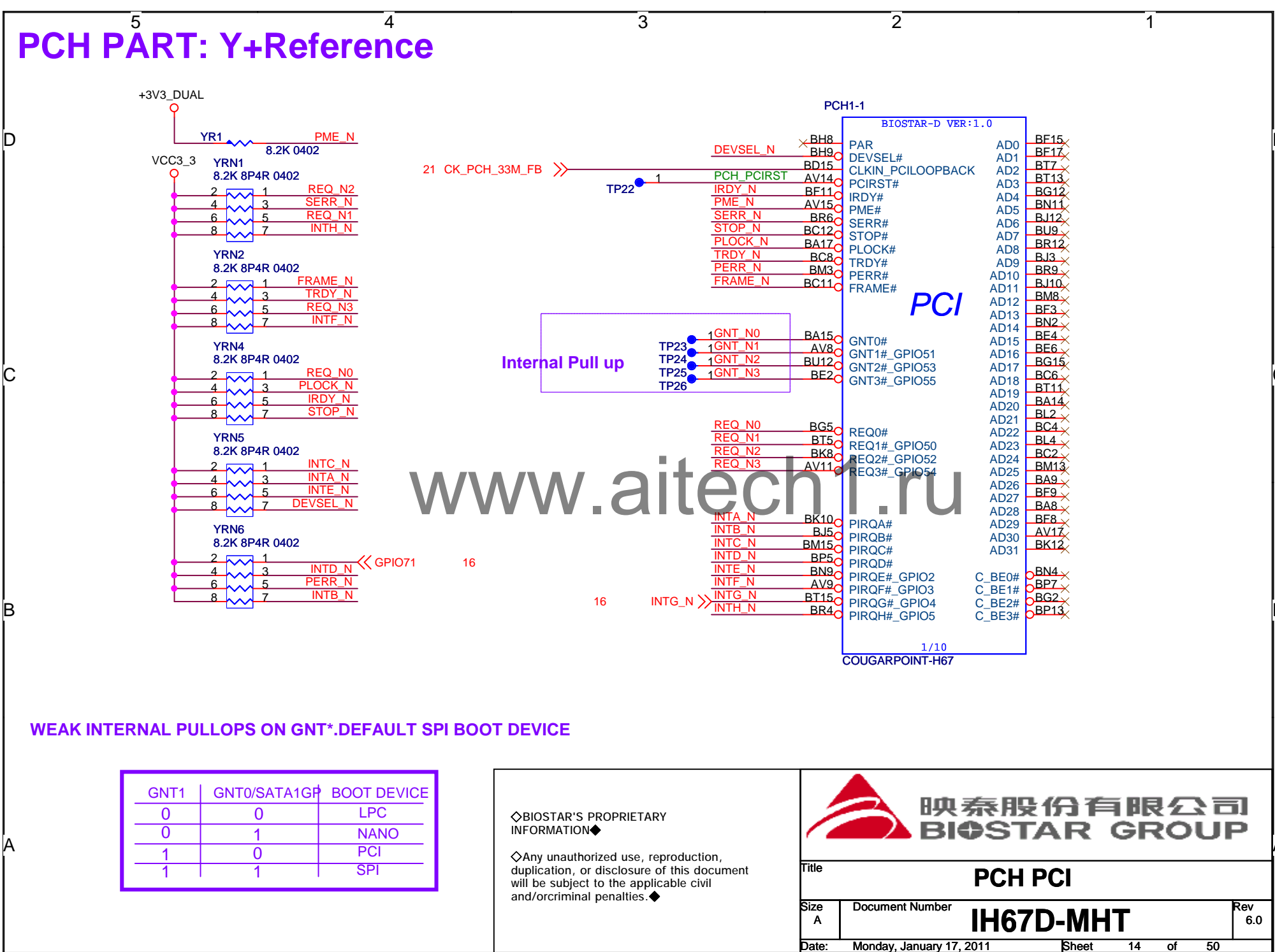
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**PCH PART: Y+Reference**

**Schematic Diagram:**

The diagram illustrates the PCH PCI interface circuitry. It shows connections between various components and pins.

**Left Side Connections:**

- +3V3\_DUAL connected to VCC3\_3.
- YR1 (8.2K 0402) connects +3V3\_DUAL to PME\_N.
- VCC3\_3 connected to YRN1 (8.2K 8P4R 0402), which connects to REQ\_N2, SERR\_N, REQ\_N1, and INTN\_N.
- YRN2 (8.2K 8P4R 0402) connects to FRAME\_N, TRDY\_N, REQ\_N3, and INTF\_N.
- YRN4 (8.2K 8P4R 0402) connects to REQ\_N0, PLOCK\_N, IRDY\_N, and STOP\_N.
- YRN5 (8.2K 8P4R 0402) connects to INTC\_N, INTA\_N, INTE\_N, and DEVSEL\_N.
- YRN6 (8.2K 8P4R 0402) connects to INTD\_N, PERR\_N, and INTB\_N.

**Internal Pull up:**

A box labeled "Internal Pull up" contains TP23, TP24, TP25, and TP26, which are connected to GNT\_N0, GNT\_N1, GNT\_N2, and GNT\_N3 respectively.

**Right Side Connections:**

- DEVSEL\_N connected to BH8 and BH9.
- PCH\_PCIRST connected to BD15 and AV14.
- IRDY\_N connected to BF11 and AV15.
- PME\_N connected to BR6 and BC12.
- SERR\_N connected to BA17 and BC8.
- STOP\_N connected to BM3 and BC11.
- PLOCK\_N connected to GNT0# and GNT1#\_GPIO51.
- TRDY\_N connected to GNT2#\_GPIO53 and GNT3#\_GPIO55.
- PERR\_N connected to REQ0# and REQ1#\_GPIO50.
- FRAME\_N connected to REQ2#\_GPIO52 and REQ3#\_GPIO54.
- REQ\_N0 connected to BG5 and BT5.
- REQ\_N1 connected to BK8 and BV11.
- REQ\_N2 connected to BK10 and BJ5.
- REQ\_N3 connected to BM15 and BP5.
- INTA\_N connected to BN9 and BV9.
- INTB\_N connected to BT15 and BR4.
- INTC\_N connected to C\_BE0# and C\_BE1#.
- INTD\_N connected to C\_BE2# and C\_BE3#.
- INTE\_N connected to BN4 and BP7.
- INTF\_N connected to BG2 and BP13.
- INTG\_N connected to INTG\_N.
- INTH\_N connected to INTG\_N.

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**COUGARPOINT-H67**

**Table:**

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
0	1	NANO
1	0	PCI
1	1	SPI

**WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE**

**Legend:**

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**Size A**

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**PCH PART: Y+Reference**

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# PCH PART: Y+Reference

D

C

B

A

WEAK INTERNAL PULLUPS ON GNT\*.DEFAULT SPI BOOT DEVICE

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
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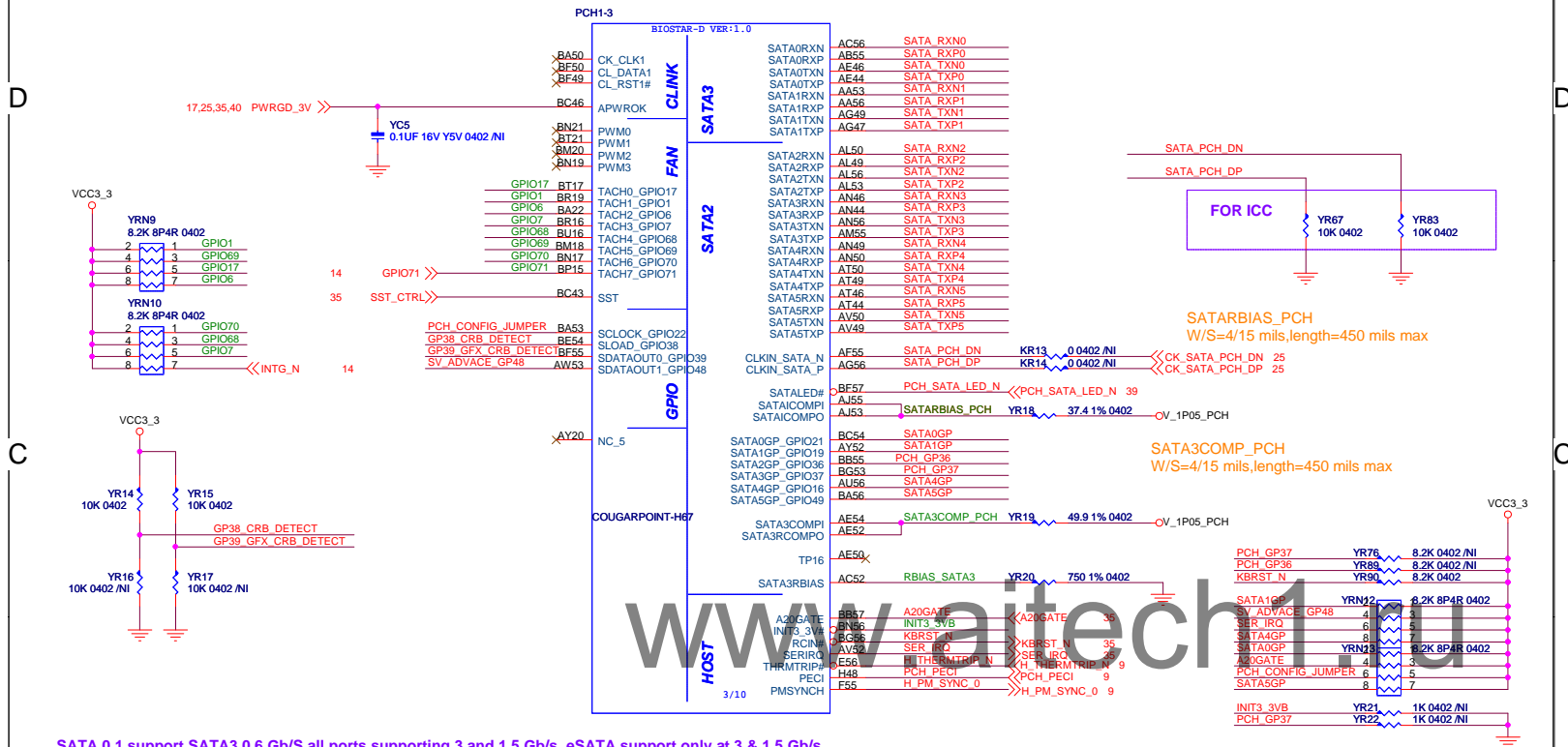
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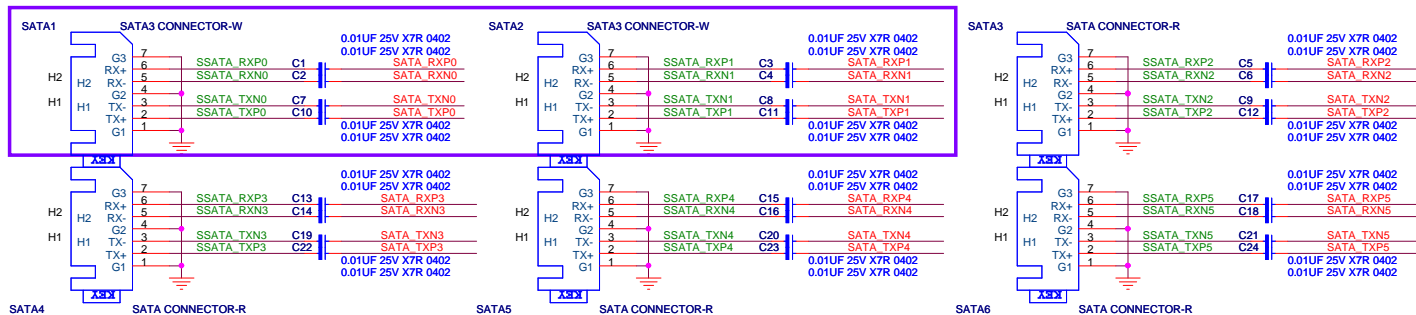
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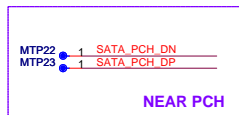
# PCH PART: Y+Reference



SATA 0,1 support SATA3.0,6 Gb/S,all ports supporting 3 and 1.5 Gb/s. eSATA support only at 3 & 1.5 Gb/s



Interleaved TX and RX pairs so that no RX pair is adjacent to two TX pairs



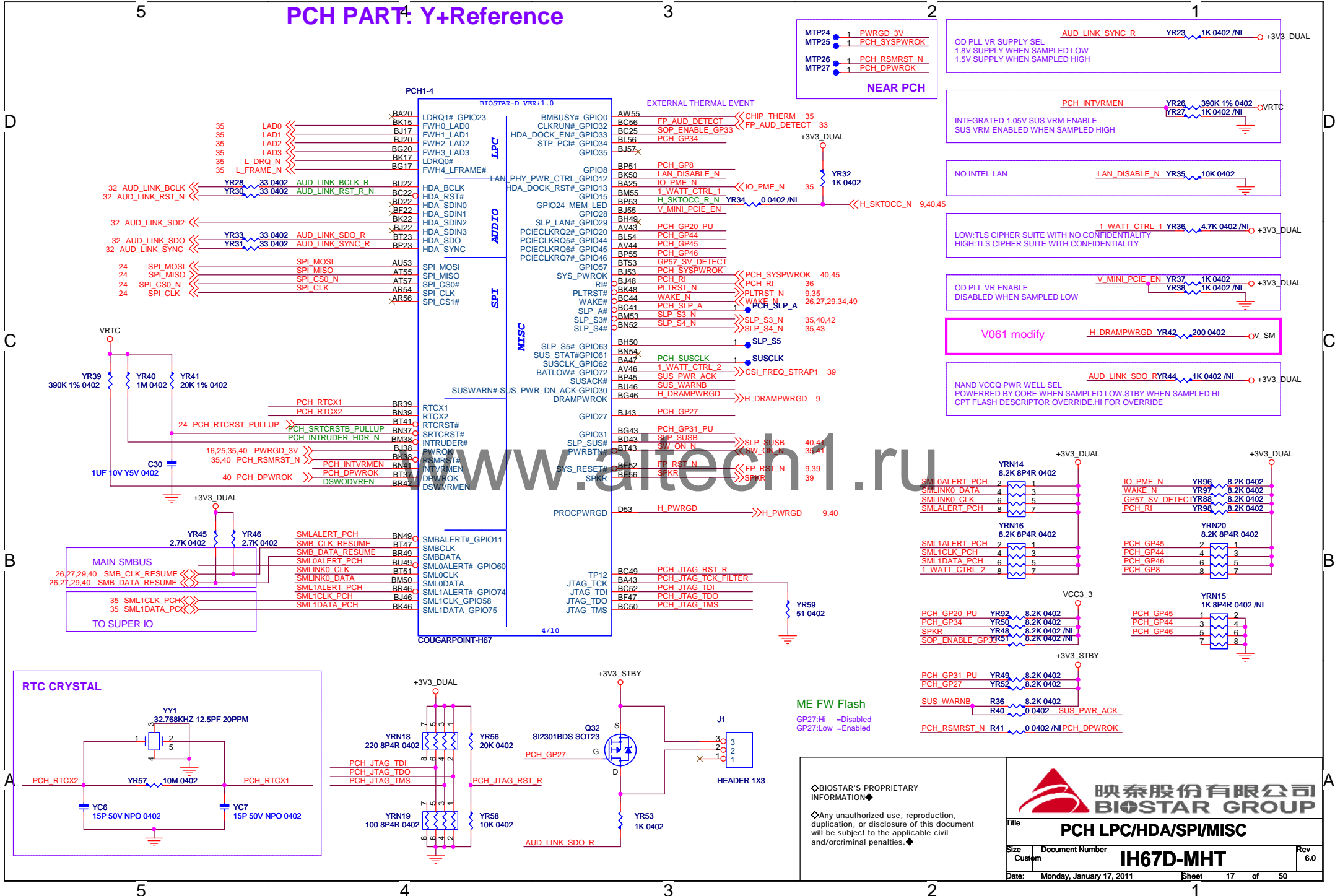
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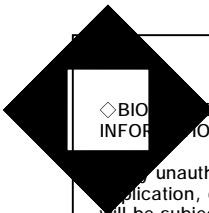
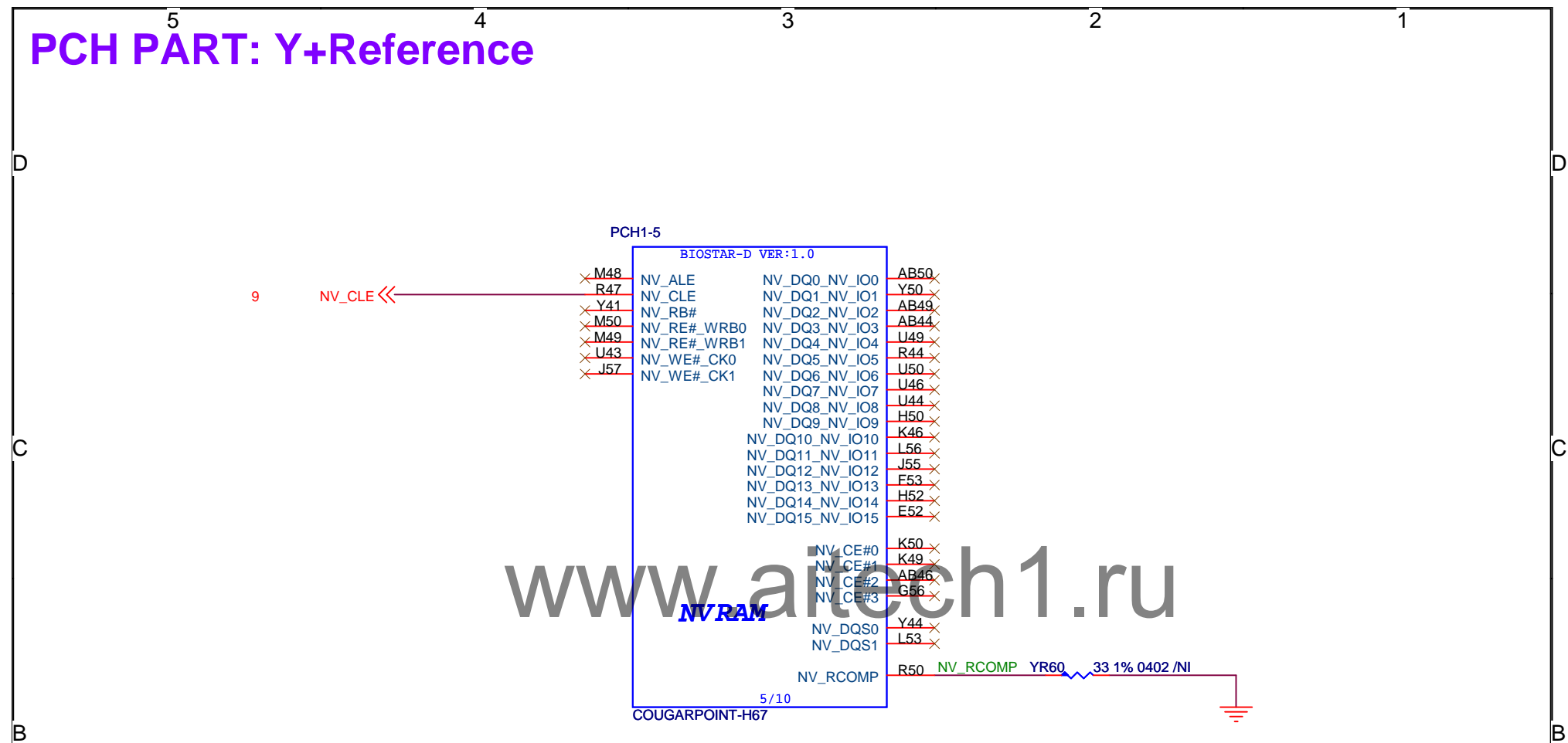


Title			PCH CLINK/SATA/CPU HOST
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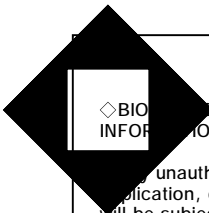
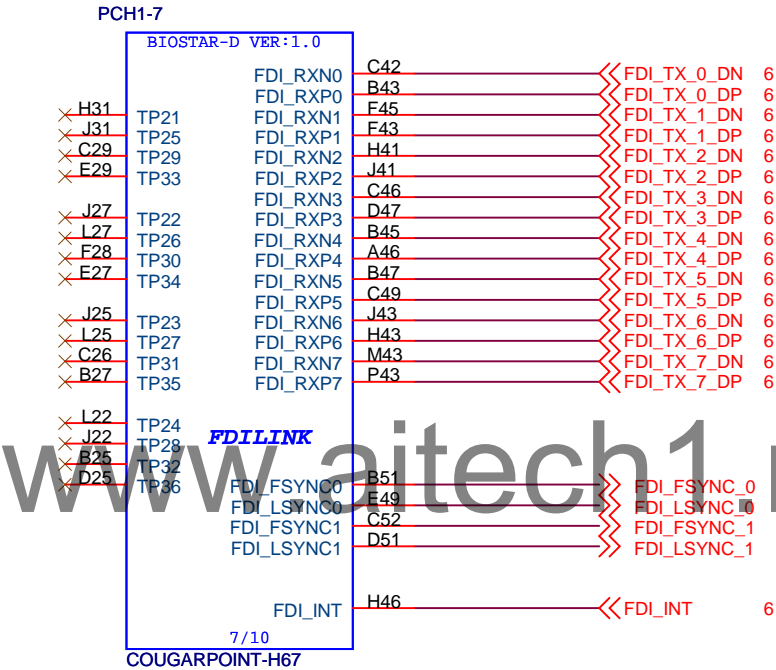
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Title PCH FDI LINK

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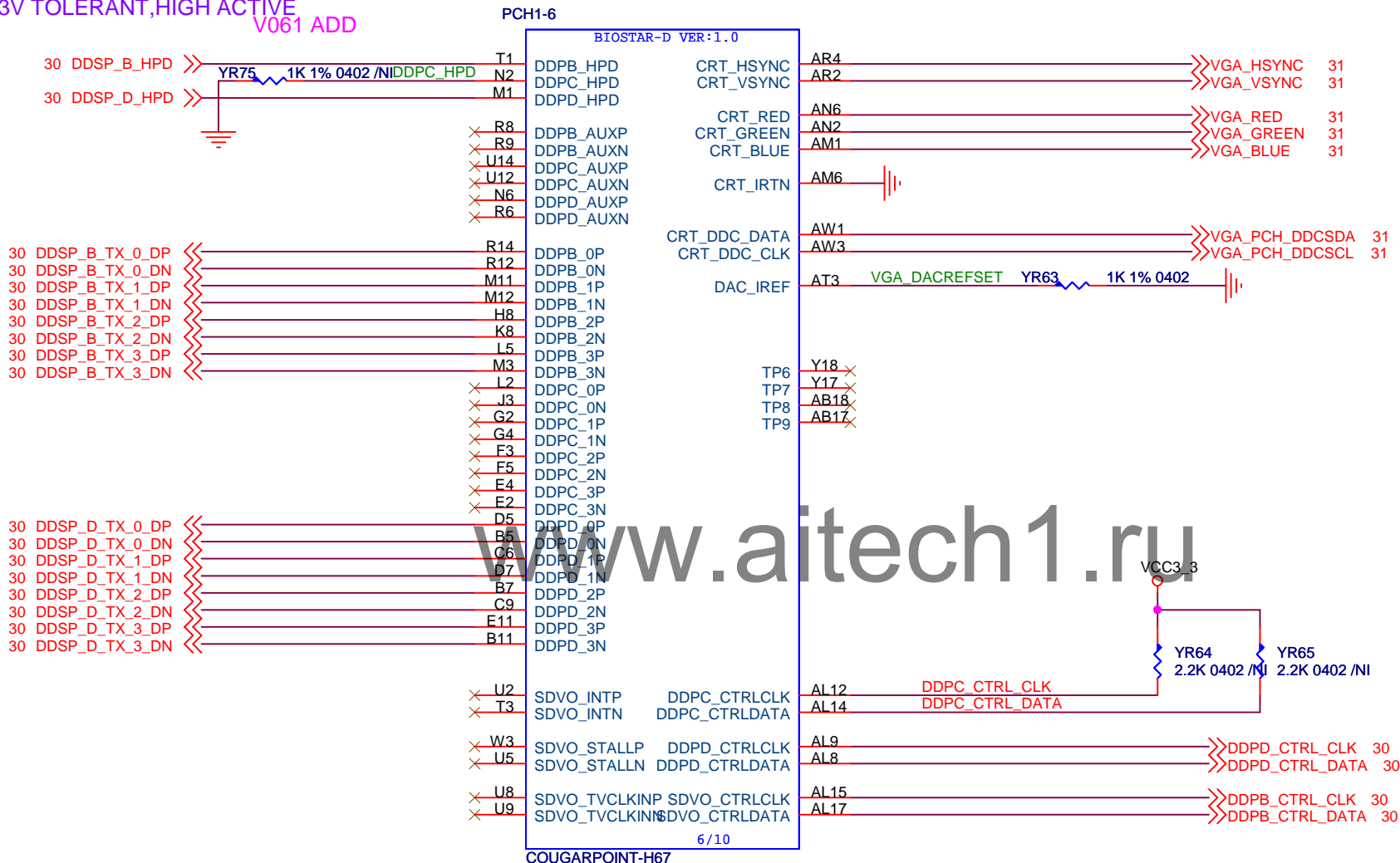
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# PCH PART: Y+Reference

3.3V TOLERANT, HIGH ACTIVE  
V061 ADD



REMOVE LEVEL SHIFTER WHEN TRACE LENGTH LESS THAN 9.25 INCHES

	FUNCTION
PORTB	DVI OR SDVO
PORTC	DISPLAY PORT
PORTD	HDMI/DVI/eDP

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Title **PCH VGA/DISPLAY PORT**

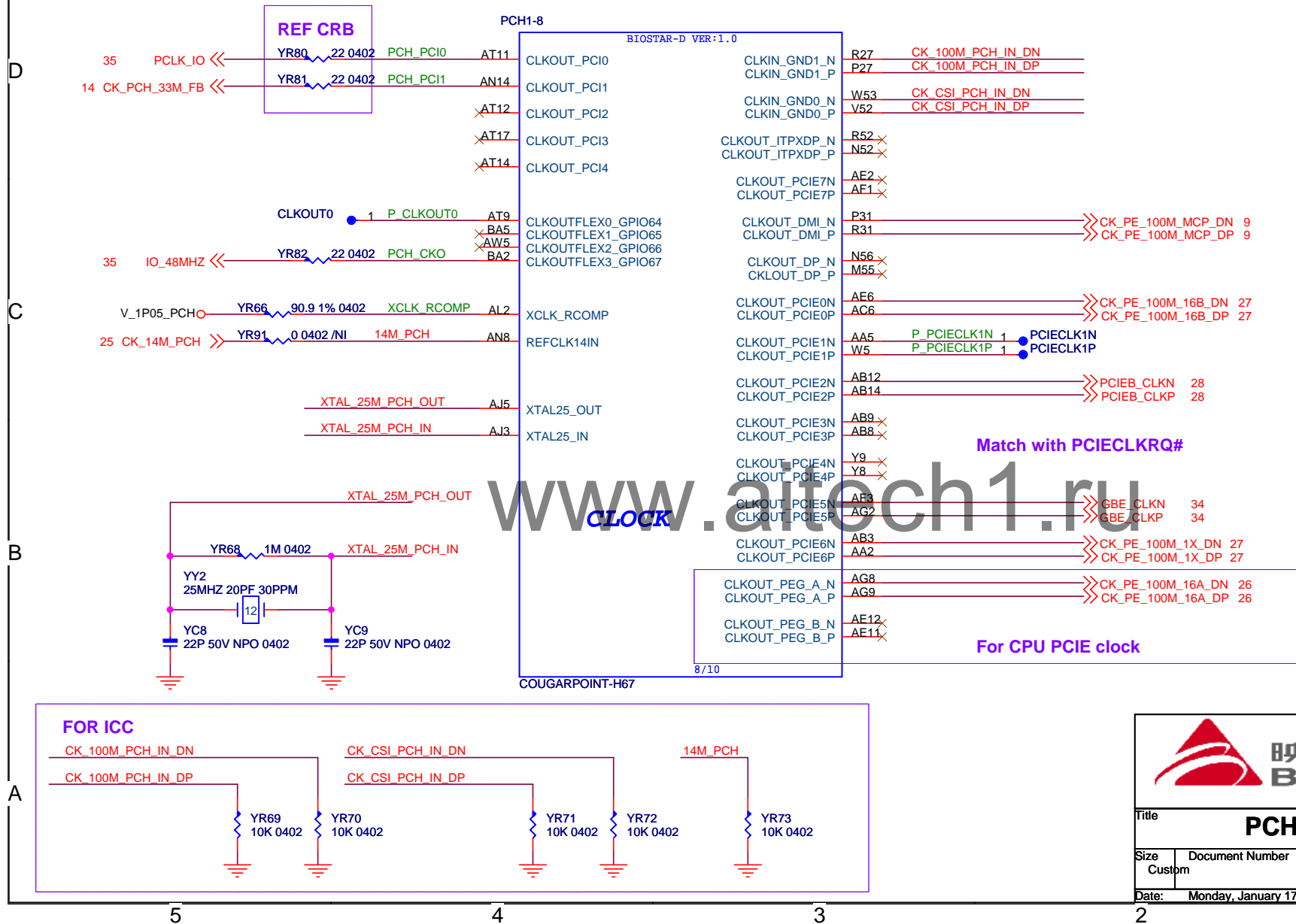
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# PCH PART: Y+Reference



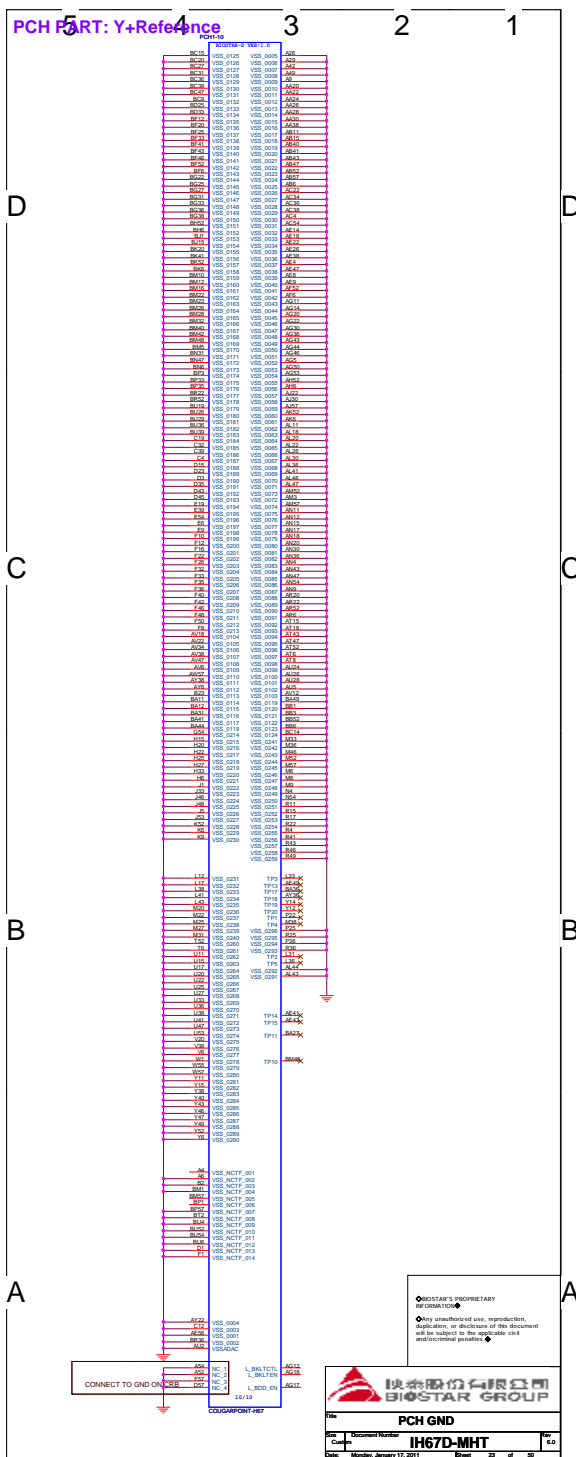
**映泰股份有限公司**  
**BIOSTAR GROUP**

**Title** PCH CLOCK BUFFER

**Size** Custom **Document Number** IH67D-MHT **Rev** 6.0

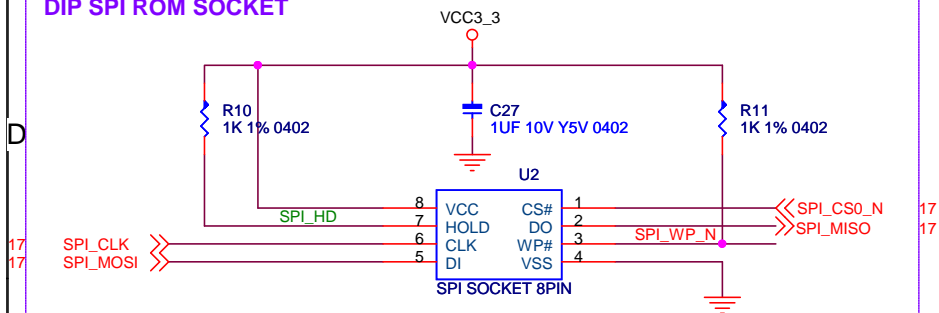
**Date:** Monday, January 17, 2011 **Sheet** 21 **of** 50



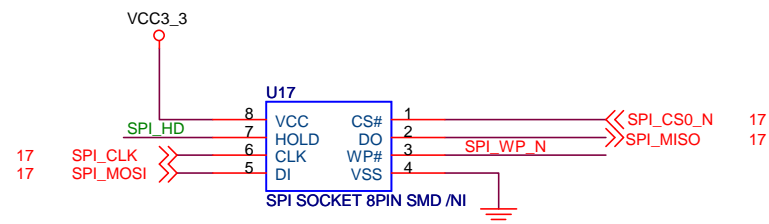


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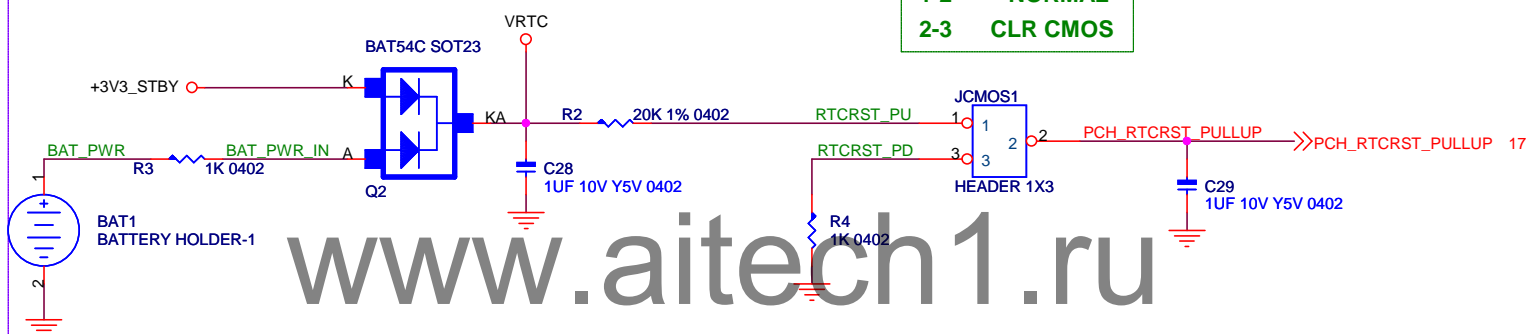
## DIP SPI ROM SOCKET



## SMD ROM SOCKET

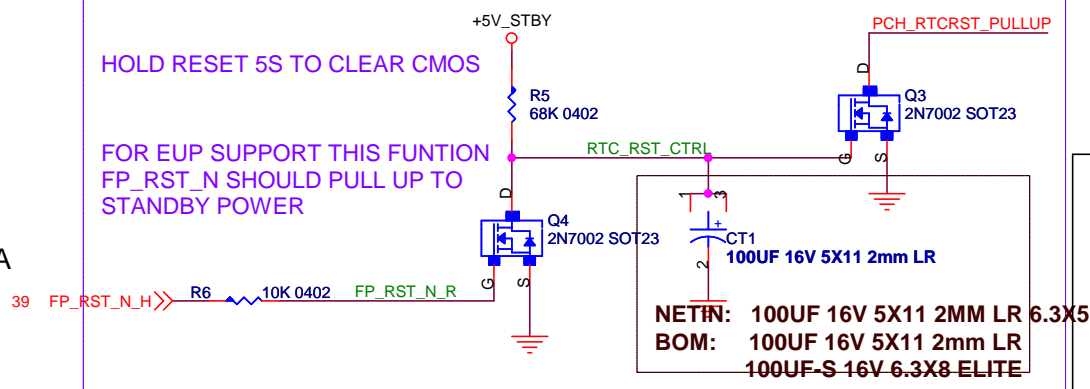


JCMOS  
1-2 NORMAL  
2-3 CLR CMOS



HOLD RESET 5S TO CLEAR CMOS

FOR EUP SUPPORT THIS FUNTION  
FP\_RST\_N SHOULD PULL UP TO  
STANDBY POWER



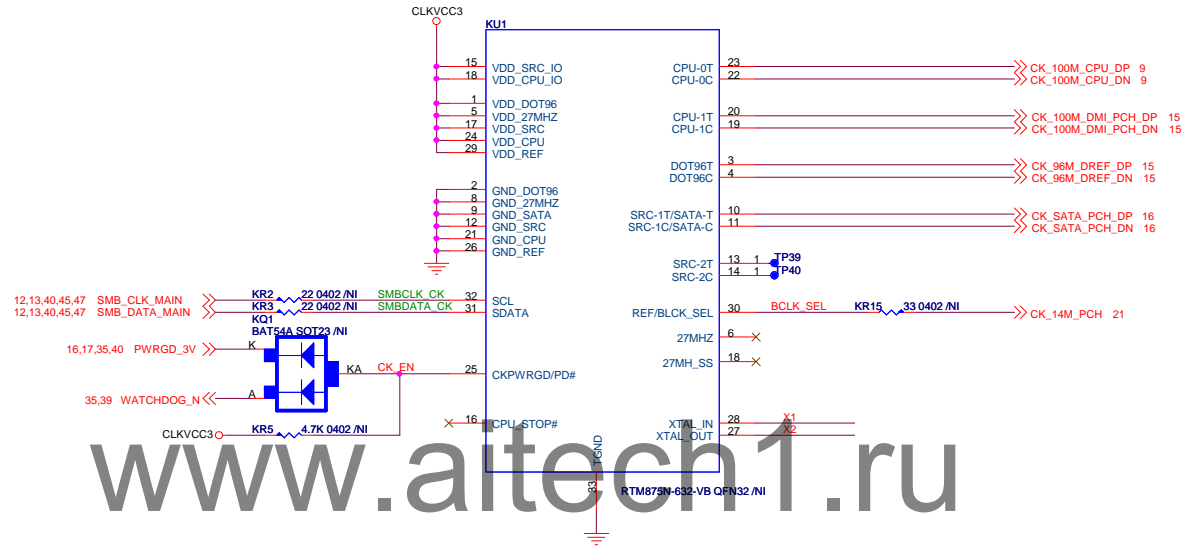
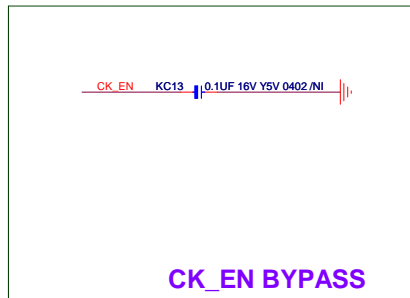
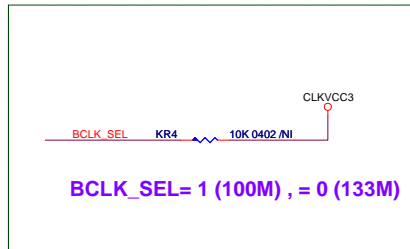
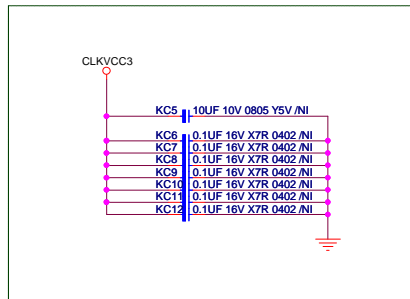
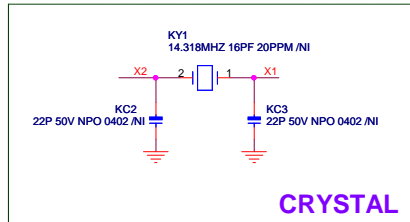
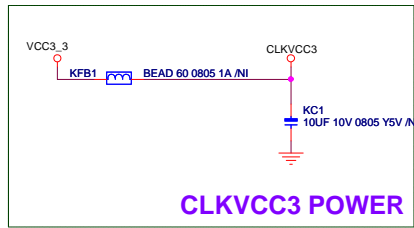
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Title			
SPI ROM/RTC CRYSTAL/BAT			
Size	Document Number	Rev	
Custom	IH67D-MHT	6.0	
Date: Monday, January 17, 2011		Sheet	24 of 50

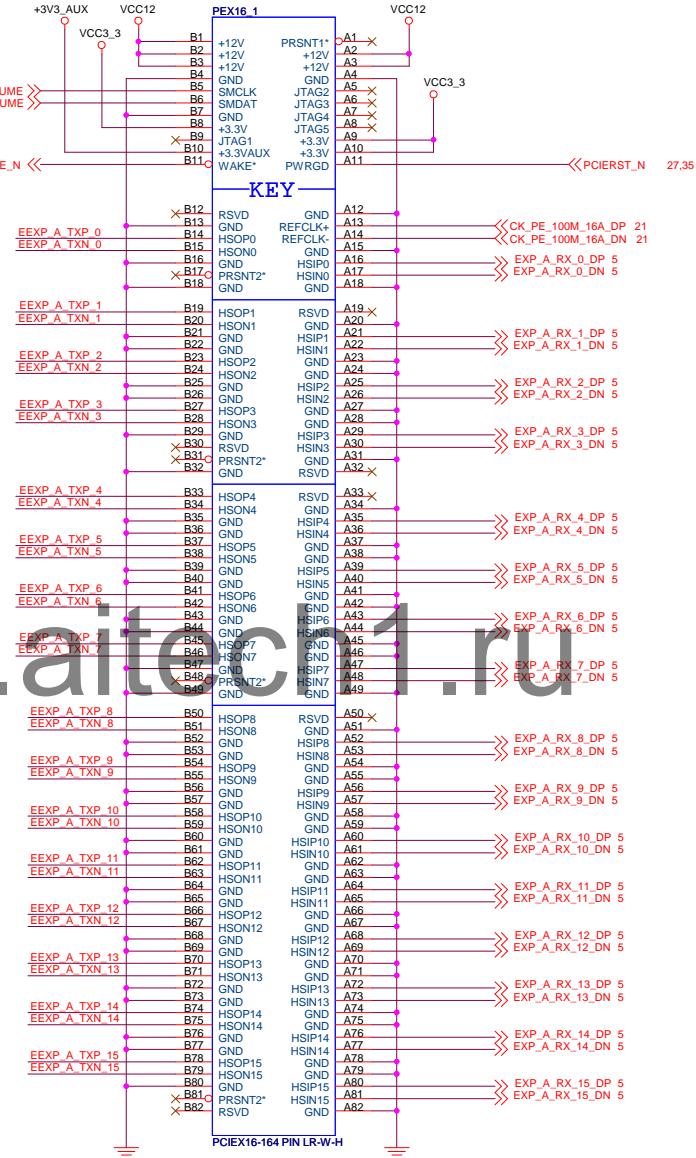
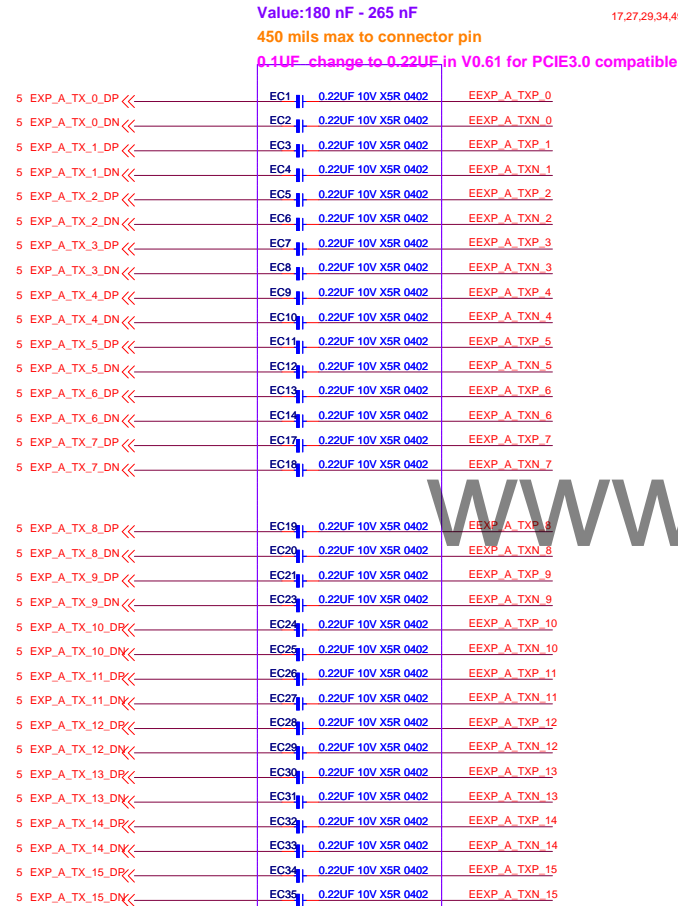
# CLOCK GEN PART: K+Reference



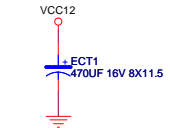
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Title CK505 CLOCK GENERATOR			
Size Custom	Document Number IH67D-MHT		Rev 6.0
Date	Monday, January 17, 2011	Sheet	25 of 50

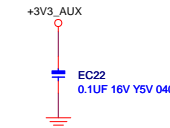
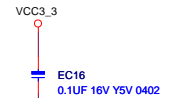
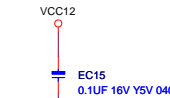
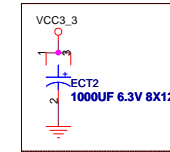
# SLOT PART: E+Reference



For ALL SOLID-----270UF-S 16V 8X11 ELITE  
For NO SOLID-----470UF 16V 8X11.5



NETIN:560UF-S 6.3V 6.3X8 8X8  
BOM: 1000UF 6.3V 8X12  
560UF-S 6.3V 6.3X8 ELITE

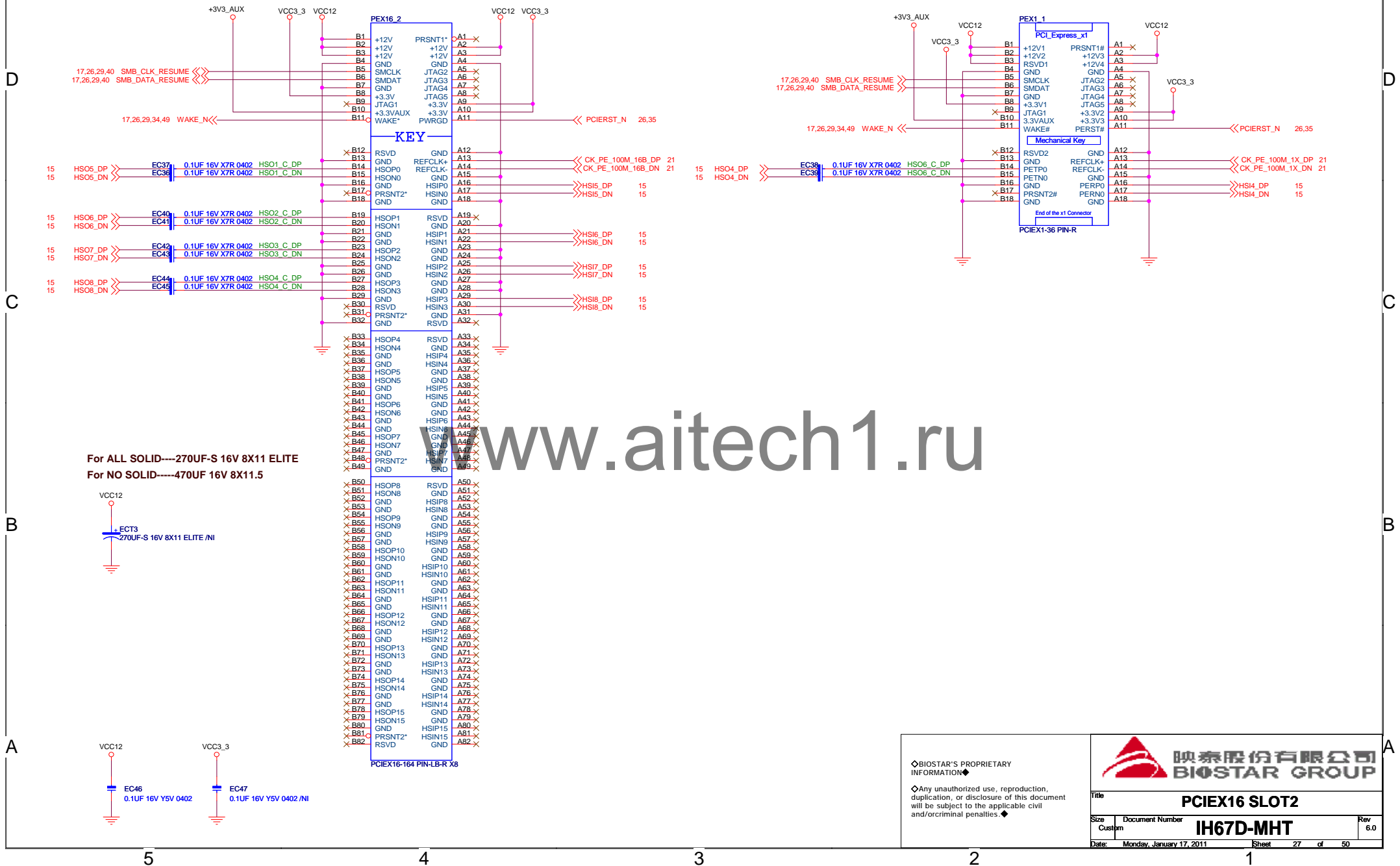


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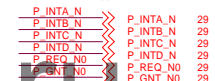
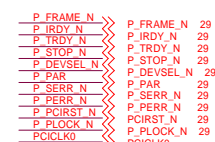
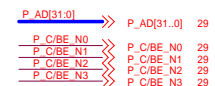
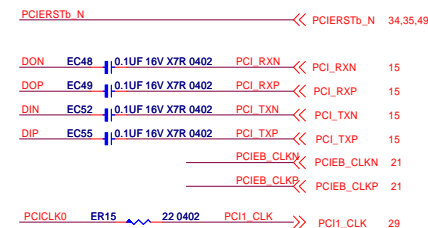
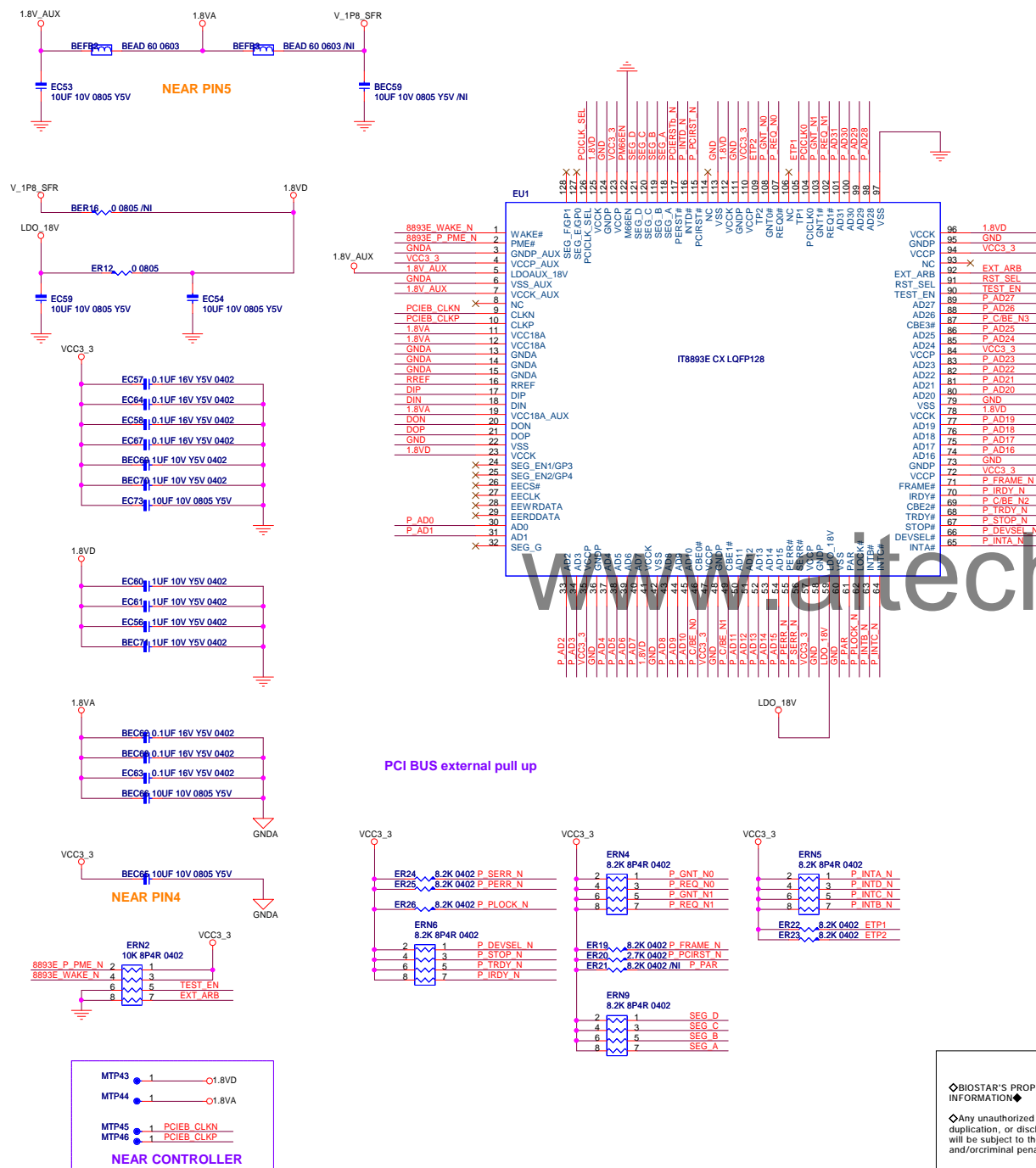
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Title <b>PCIE16 SLOT1</b>	
Size Custom	Document Number <b>IH67D-MHT</b>
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Rev 6.0	

# SLOT PART: E+Reference



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<b>Title</b> PCIEX16 SLOT2			
<b>Size</b> Custom	<b>Document Number</b> IH67D-MHT	<b>Rev</b> 6.0	
<b>Date</b> Monday, January 17, 2011		<b>Sheet</b> 27 of 50	

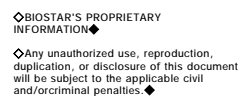
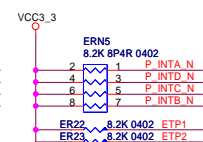
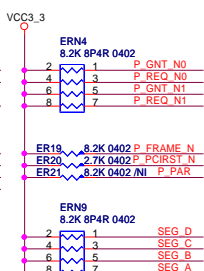
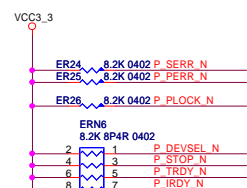
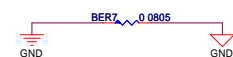
## SLOT PART: E+Reference



M66EN = LOW : DISABLED



### Close to Chip

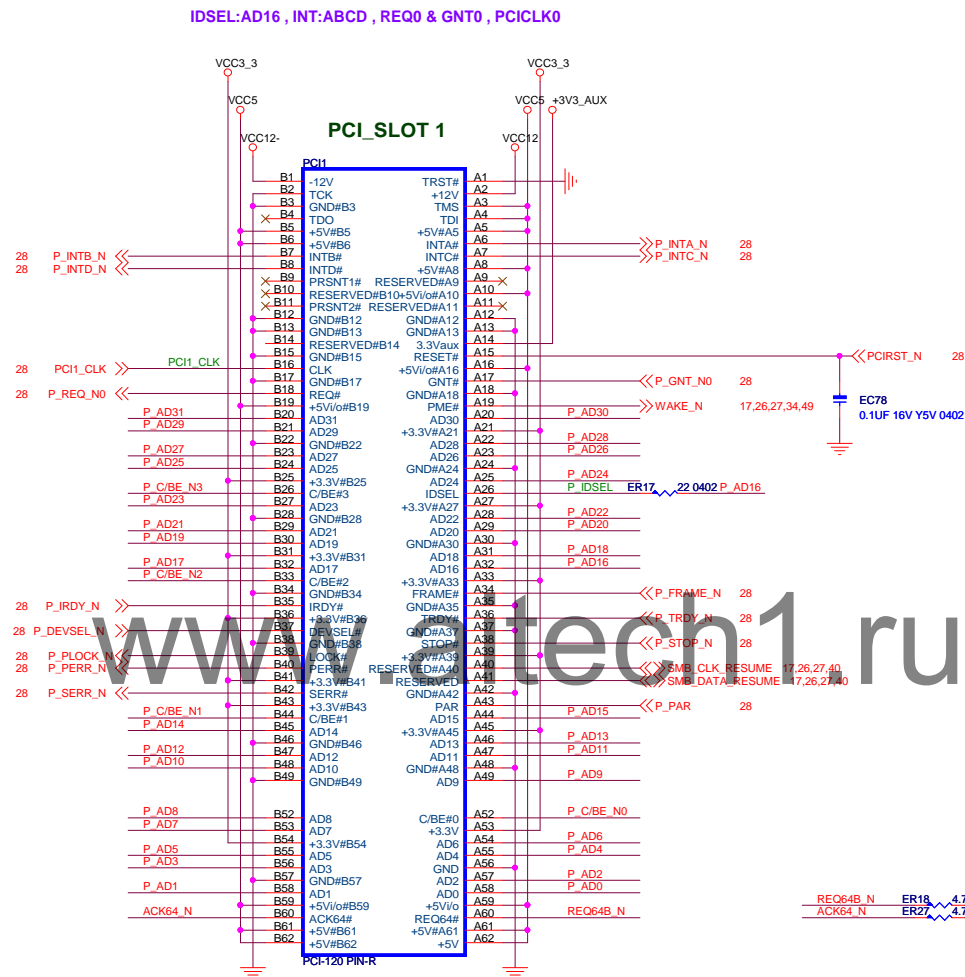


Title	PCI BRIDGE IT8893
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Size Custom	Document Number <b>IH67D-MHT</b>	Rev 6.0
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# SLOT PART: E+Reference

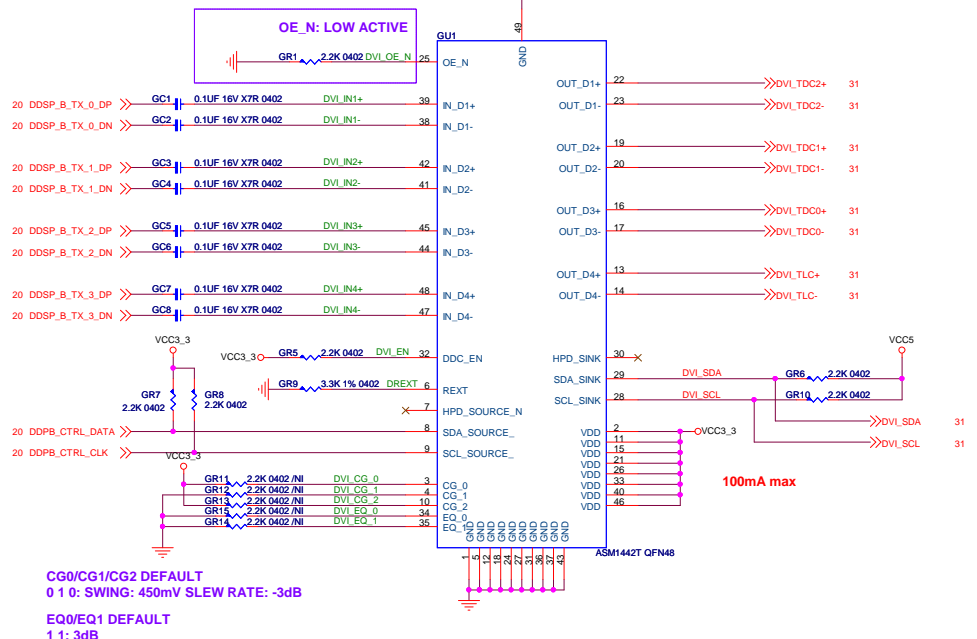


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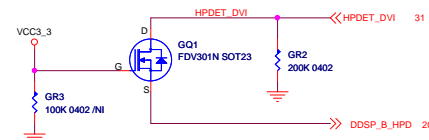
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Size	Document Number	<b>IH67D-MHT</b>	
Date:	Monday, January 17, 2011	Sheet	29 of 50
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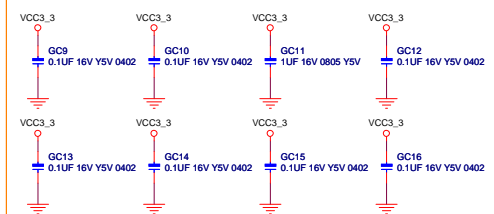
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For 1442T, RESERVE THIS CIRCUIT

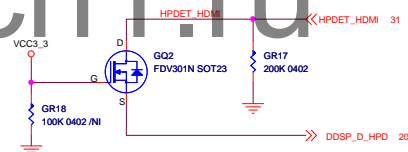


CLOSE TO GU1 VDD PIN

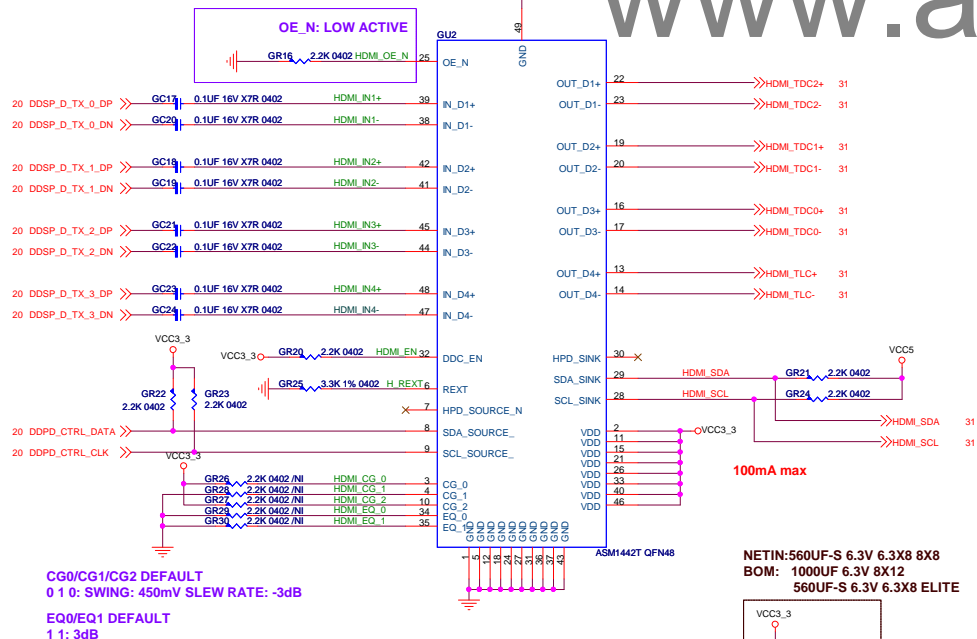
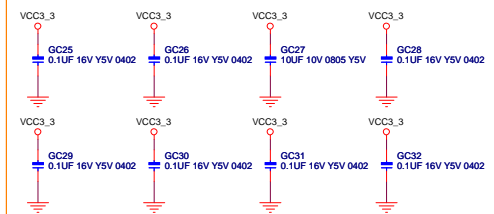


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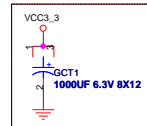
For 1442T, RESERVE THIS CIRCUIT



CLOSE TO GU2 VDD PIN



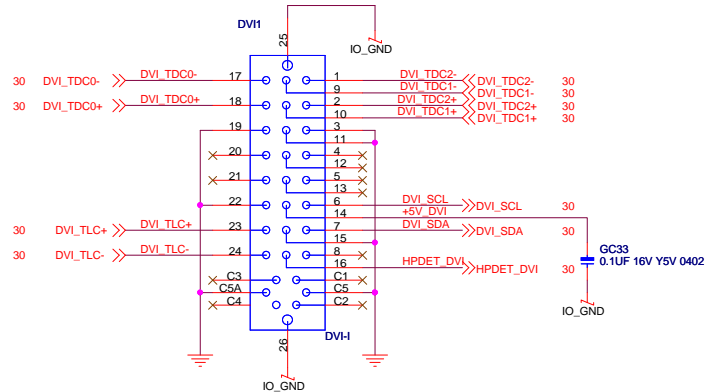
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BOM: 1000UF 6.3V 8X12  
560UF-S 6.3V 6.3X8 ELITE



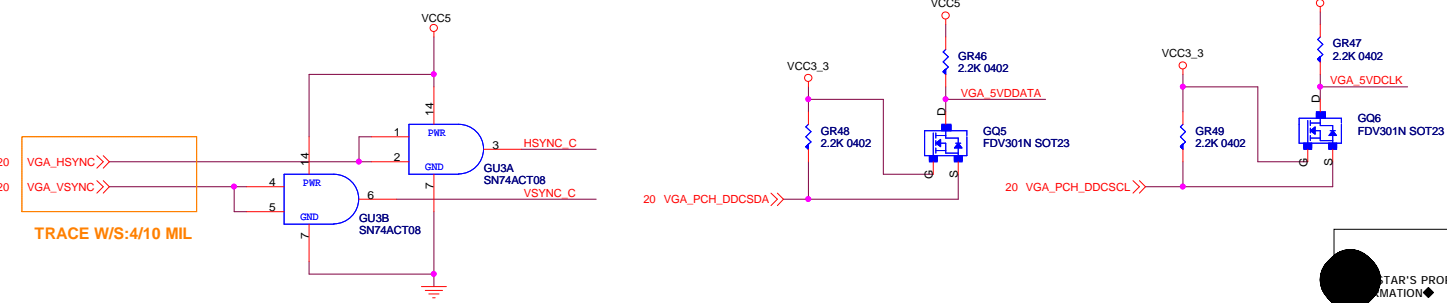
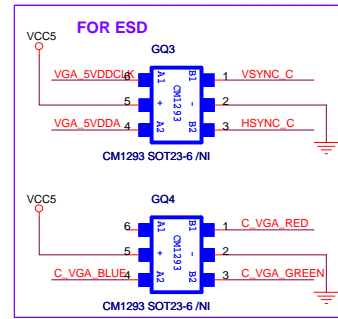
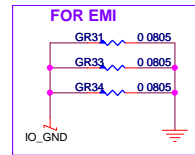
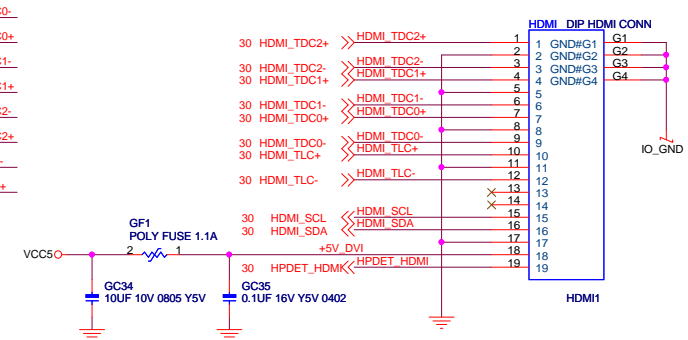
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Title	
ASM1442T LEVEL SHIFTER	
Size	Document Number
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DVI CONNECTOR  
DVI CONNECTOR TYPE ACCORD WITH SPEC



GR62	100 % 0402 /NI	HDMI TDC0- HDMI TDC0+
GR63	100 % 0402 /NI	HDMI TDC1- HDMI TDC1+
GR64	100 % 0402 /NI	HDMI TDC2- HDMI TDC2+
GR65	100 % 0402 /NI	HDMI TLC- HDMI TLC+

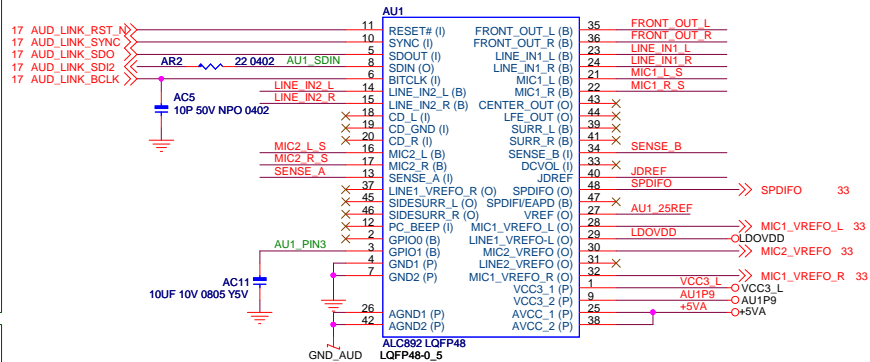
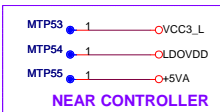
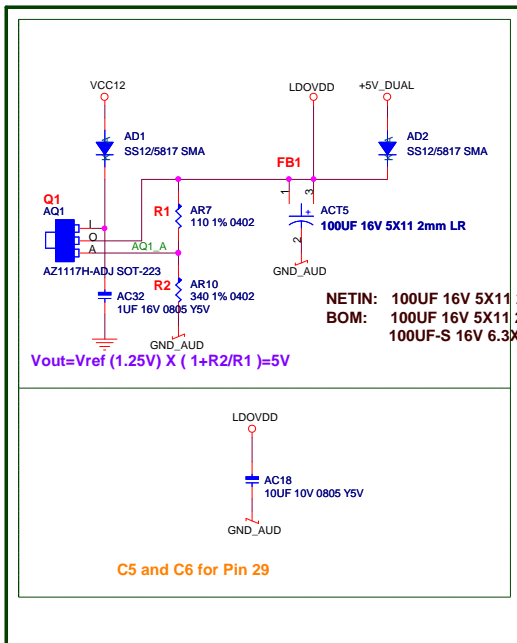
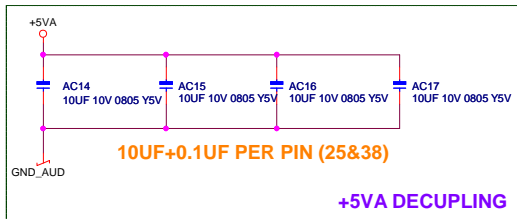
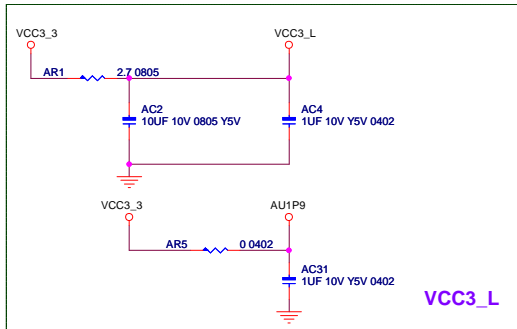


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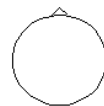
## AUDIO PART: A+Reference



## 7.1SPEAKER CONFIGURATION



SIDE-L



CEN



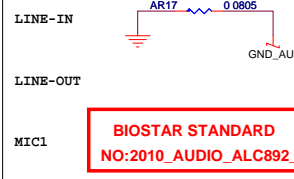
SIDE-R



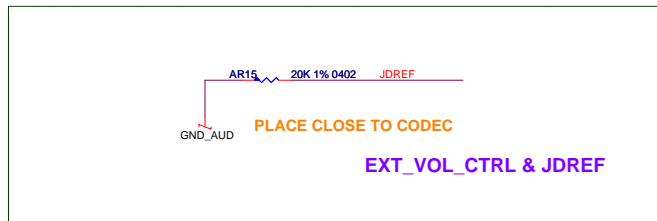
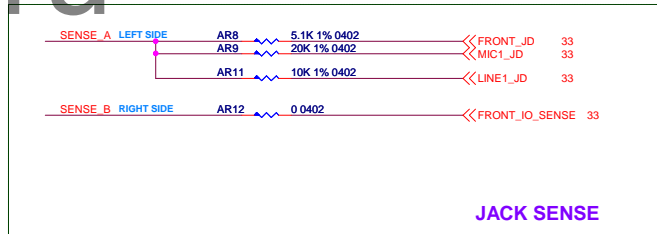
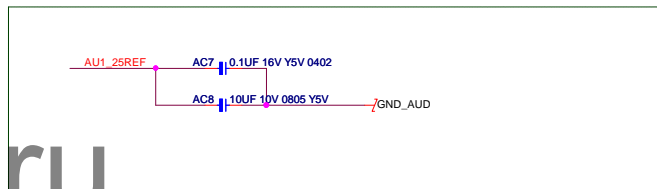
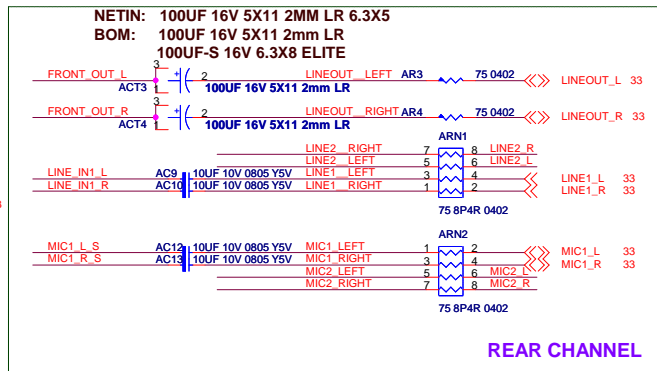
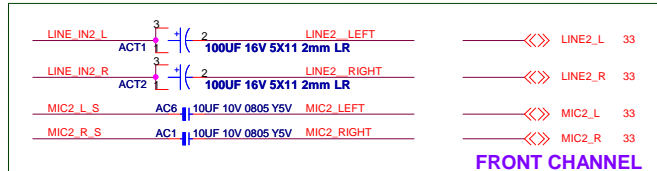
SURR-L



SURR-R



BIOSTAR STANDARD  
NO:2010\_AUDIO\_ALC892\_01



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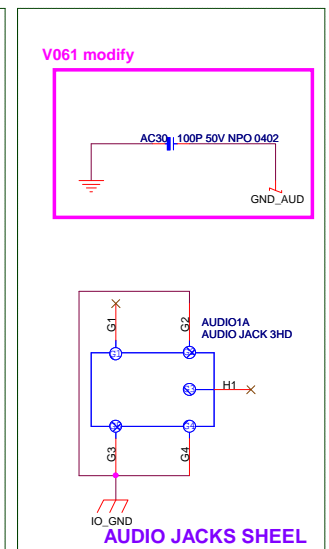
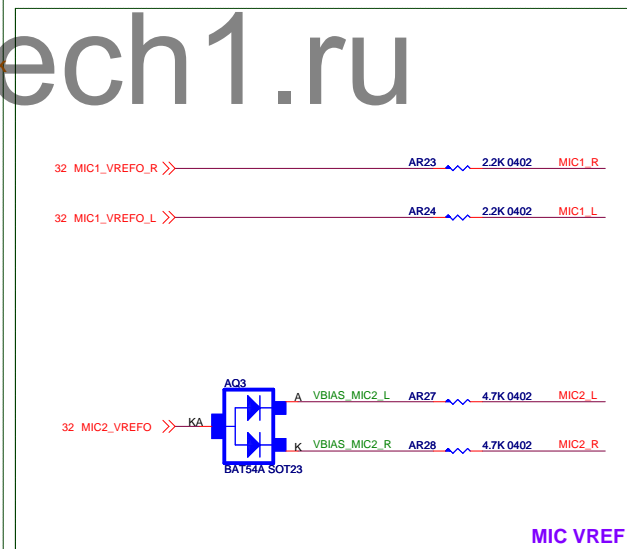
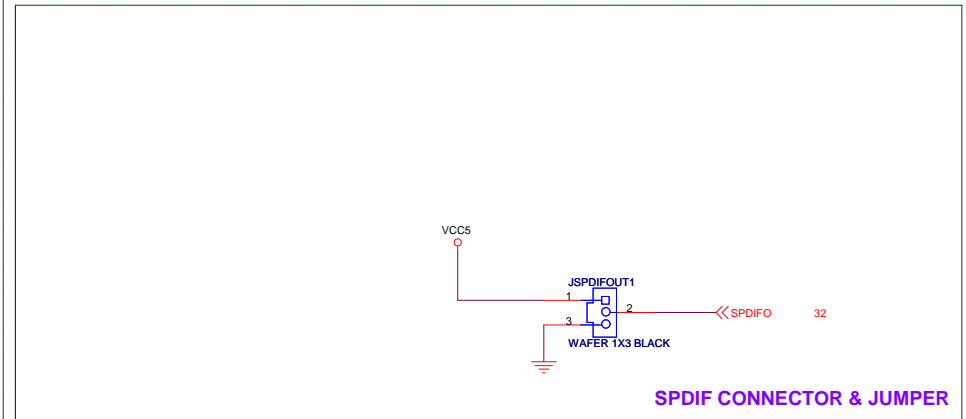
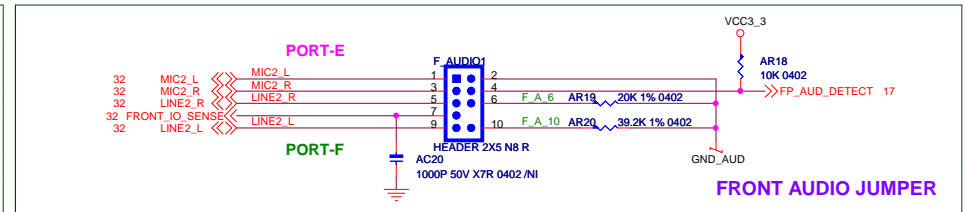
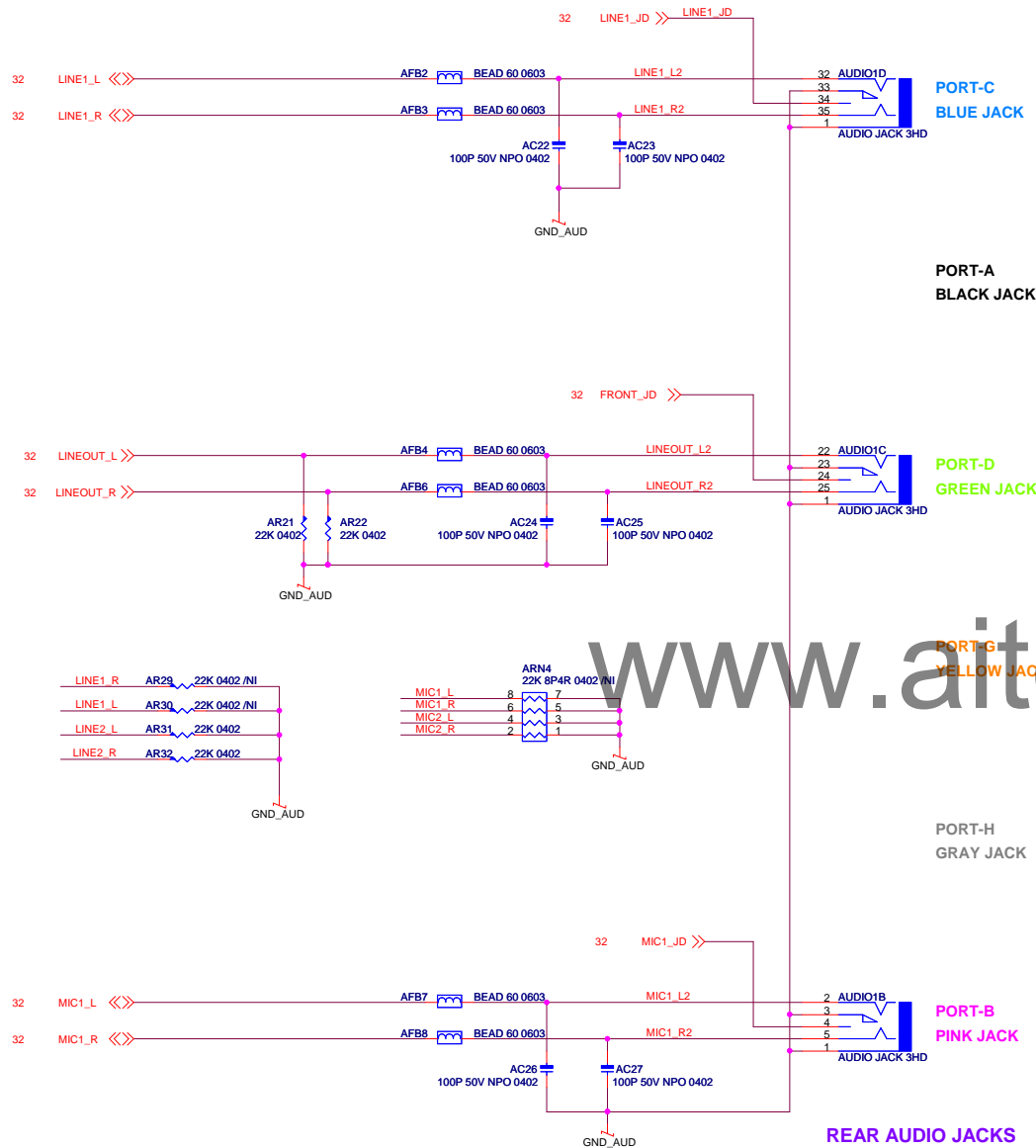
Title  
**CODEC ALC 892**

Size Custom  
Document Number  
**IH67D-MHT**

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# AUDIO PART: A+Reference



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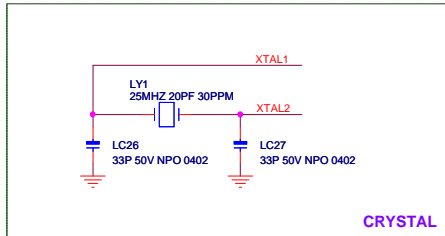
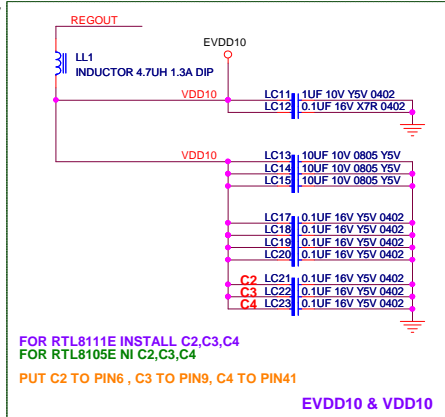
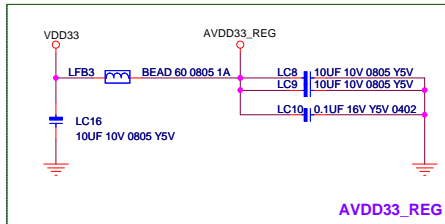
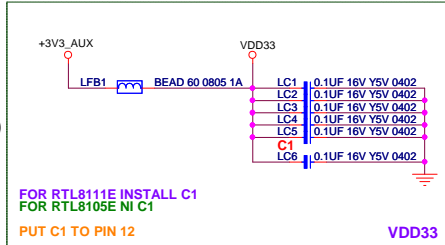
**AUDIO CONNECTOR**

**IH67D-MHT**

Rev 6.0

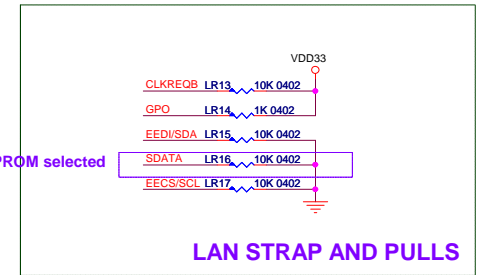
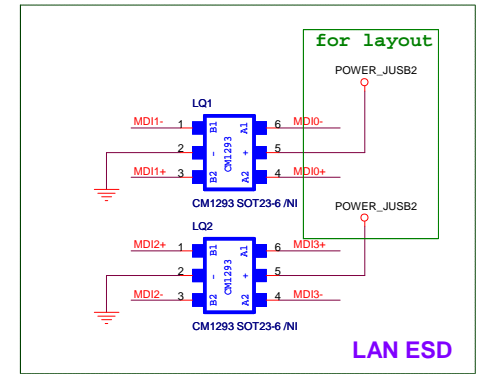
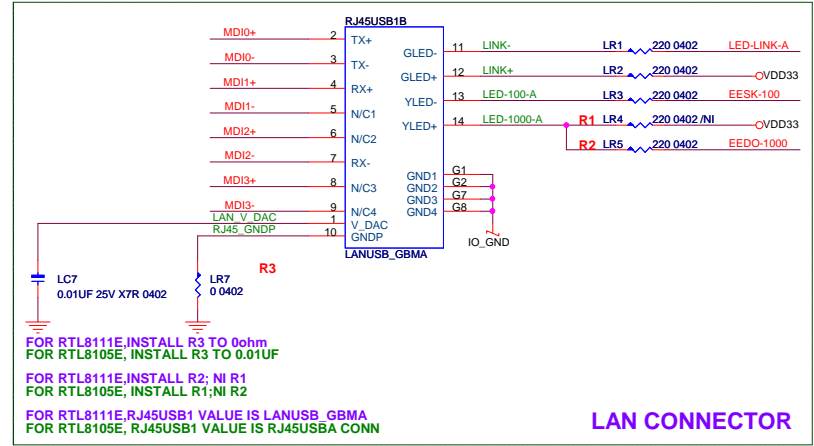
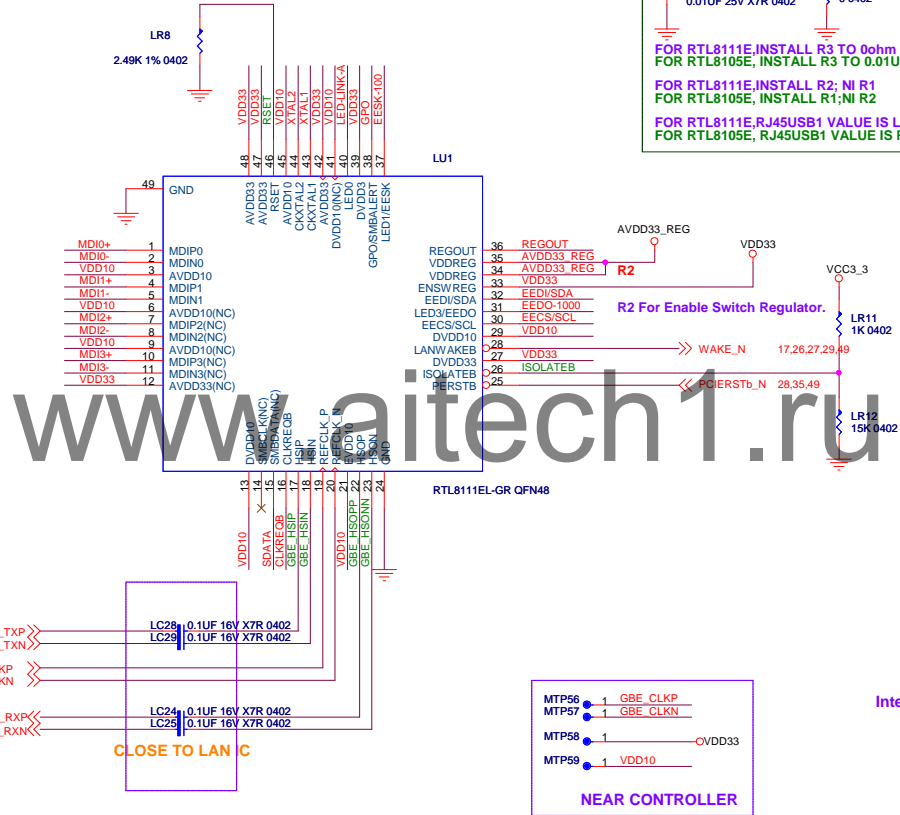
Size	Custom	Document Number	Date
		<b>IH67D-MHT</b>	Monday, January 17, 2011
		Sheet 33 of 50	

## LAN PART: L+Reference



### COMPONENT CONTRAST LIST

LAN PARTS	C1	C2	C3	C4	R1	R2	R3	RJ45 CONN
RTL8111E	O	O	O	O	X	O	0ohm	LANUSB_GBMA
RTL8105E	X	X	X	X	O	X	0.01uF	RJ45USBA CONN



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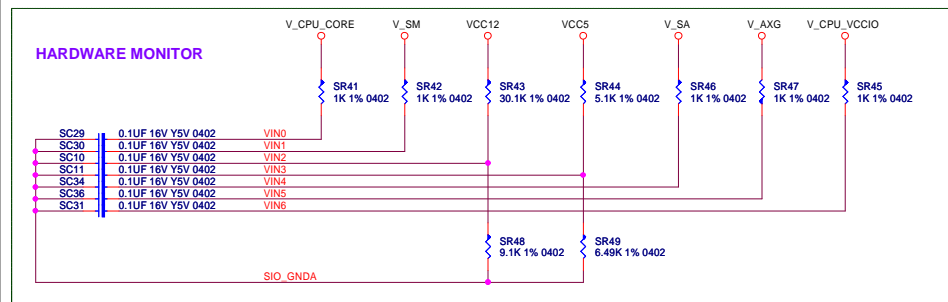
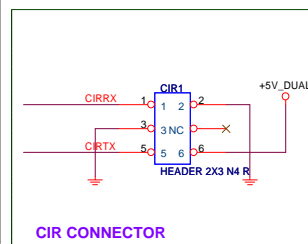
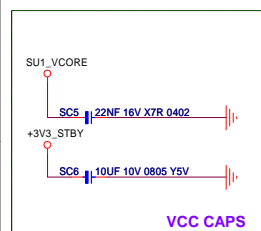
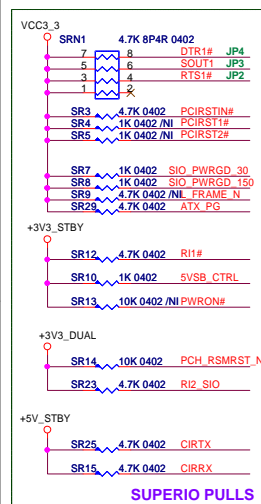
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Title: **ALC 8111E/8105E**

Size: Custom Document Number: **IH67D-MHT** Rev: 6.0

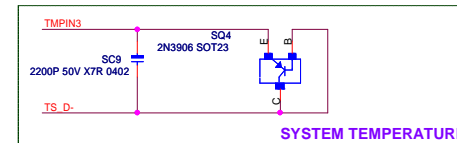
Date: Monday, January 17, 2011 Sheet: 34 of 50

# SUPERIO PART: S+Reference

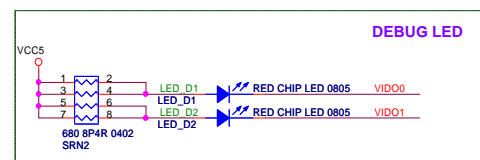


GP10,20~27,40,42~44,53~55 powered by VQCH

IT8728FBX



LED_D2	LED_D1	MESSAGE
OFF	OFF	ABNORMAL
OFF	ON	MEMORY ERROR
ON	OFF	VGA ERROR
ON	ON	NORMAL



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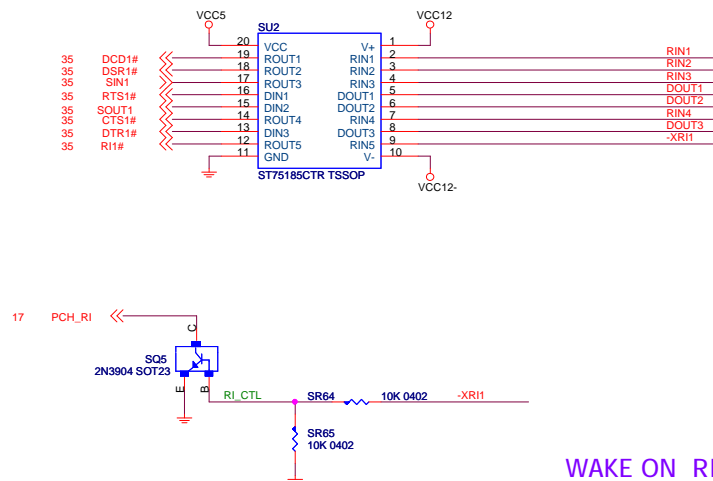
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BIOSTAR GROUP

File: SUPER I/O ITE 8728BX

Size: Custom Document Number: IH67D-MHT Rev: 6.0

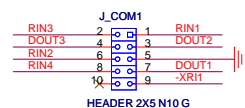
Date: Monday, January 17, 2011 Sheet: 35 of 50

## AUDIO PART: A+Reference



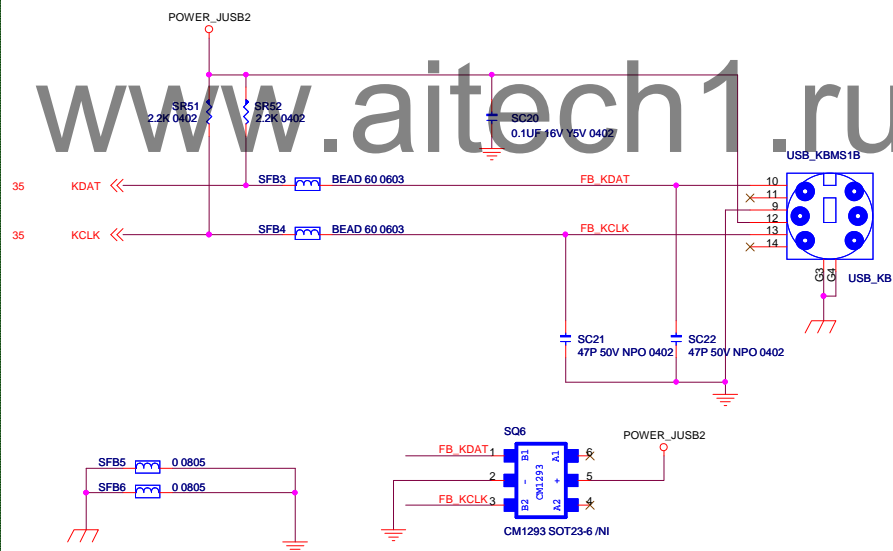
WAKE ON RING

OPTIONAL



COM PORT

FLOPPY



KEYBOARD & MOUSE

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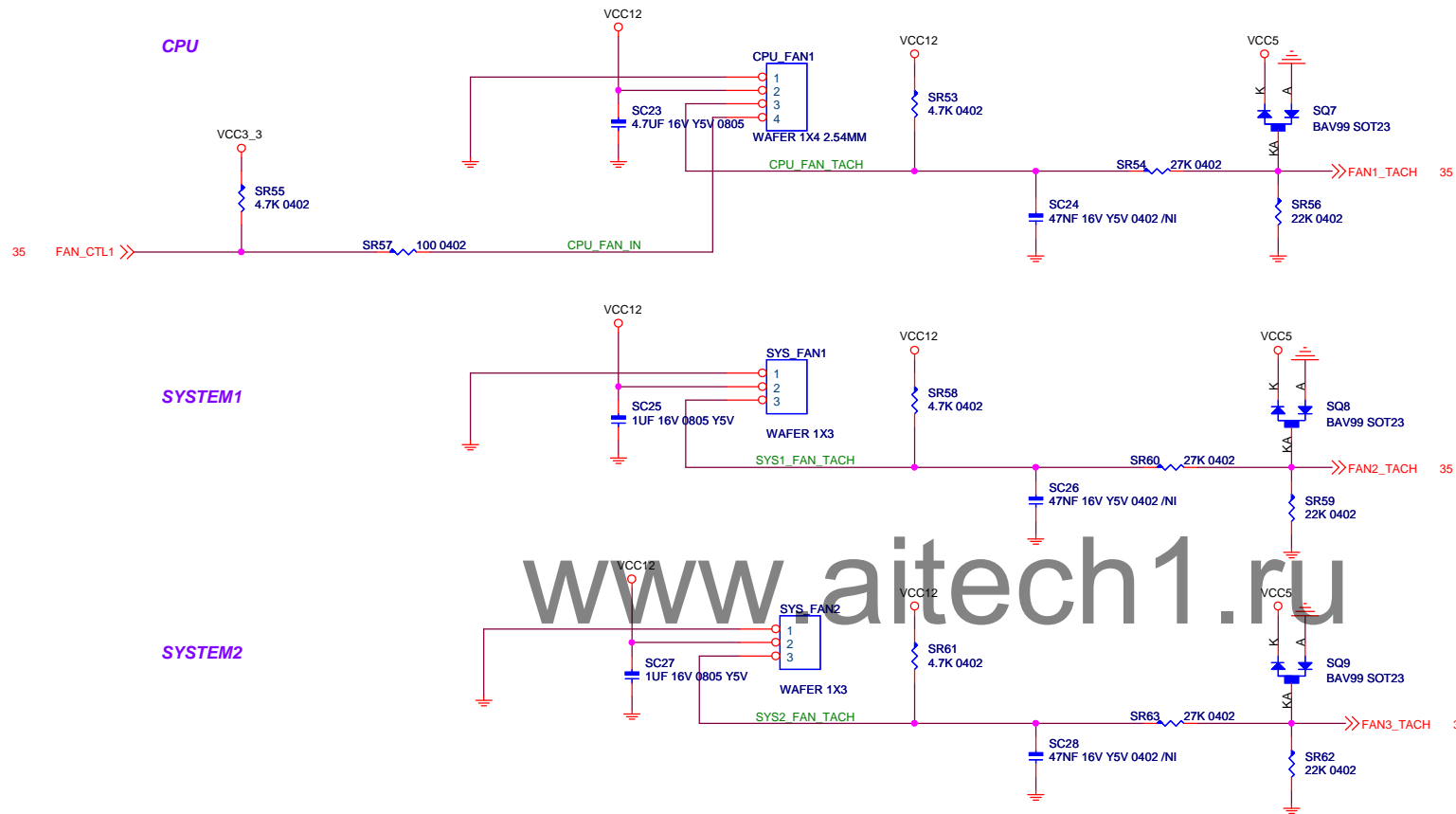


Title		
FDD / PS2 CONN		
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# AUDIO PART: A+Reference

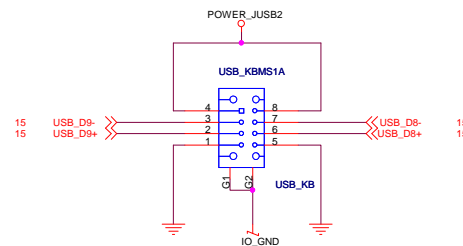
## CPU FAN/SYSTEM FAN1/SYSTEM FAN2



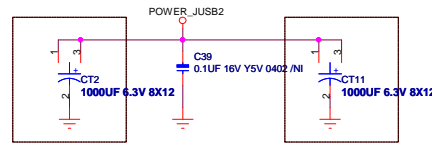
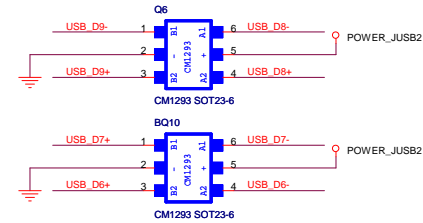
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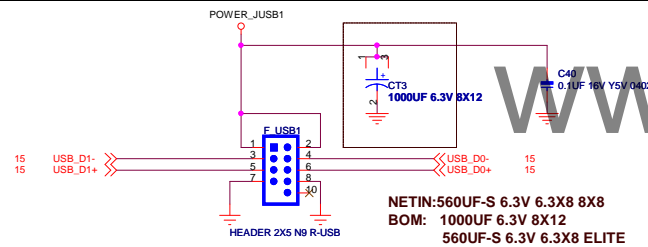
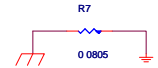
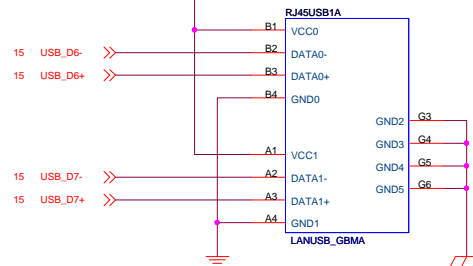
 <b>映泰股份有限公司</b> <b>BIOSTAR GROUP</b>		
<b>Title</b> <b>HW MONITOR/FAN CONTROL</b>		
<b>Size</b> Custom	<b>Document Number</b> <b>IH67D-MHT</b>	<b>Rev</b> 6.0
<b>Date:</b> Monday, January 17, 2011 <b>Sheet</b> 37 <b>of</b> 50		



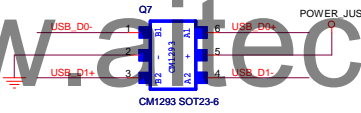
DEFAULT : 1-2 CLOSE



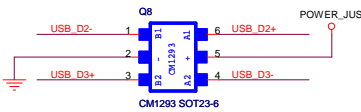
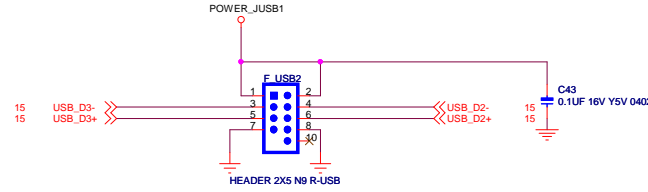
NETIN:560UF-S 6.3V 6.3X8 8X8  
BOM: 1000UF 6.3V 8X12  
560UF-S 6.3V 6.3X8 ELITE



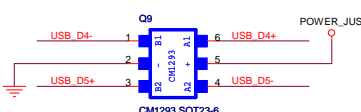
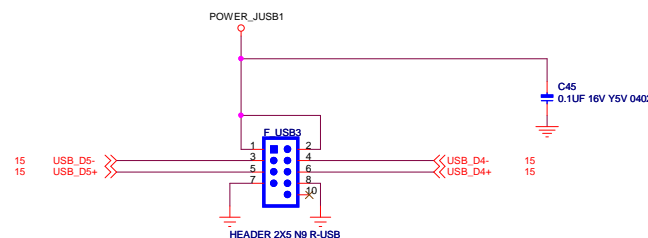
NETIN:560UF-S 6.3V 6.3X8 8X8  
BOM: 1000UF 6.3V 8X12  
560UF-S 6.3V 6.3X8 ELITE



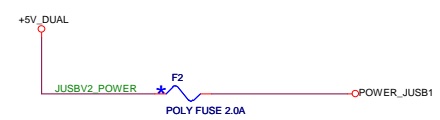
FRONT PANEL USB



FRONT PANEL USB



FRONT PANEL USB



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USB CONN	
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**FP PART: F+Reference**

**JATXPWR**

**V061 modify circuit**

**24PIN POWER CONN&FP**

**IH67D-MHT**

**Rev 6.0**

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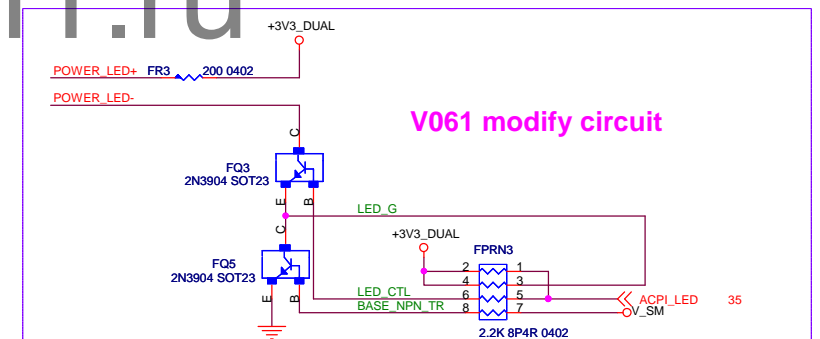
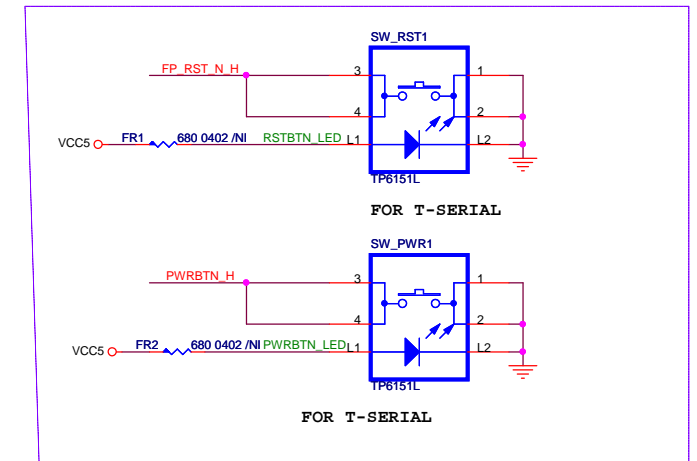
**24PIN POWER CONN&FP**

**IH67D-MHT**

**Rev 6.0**

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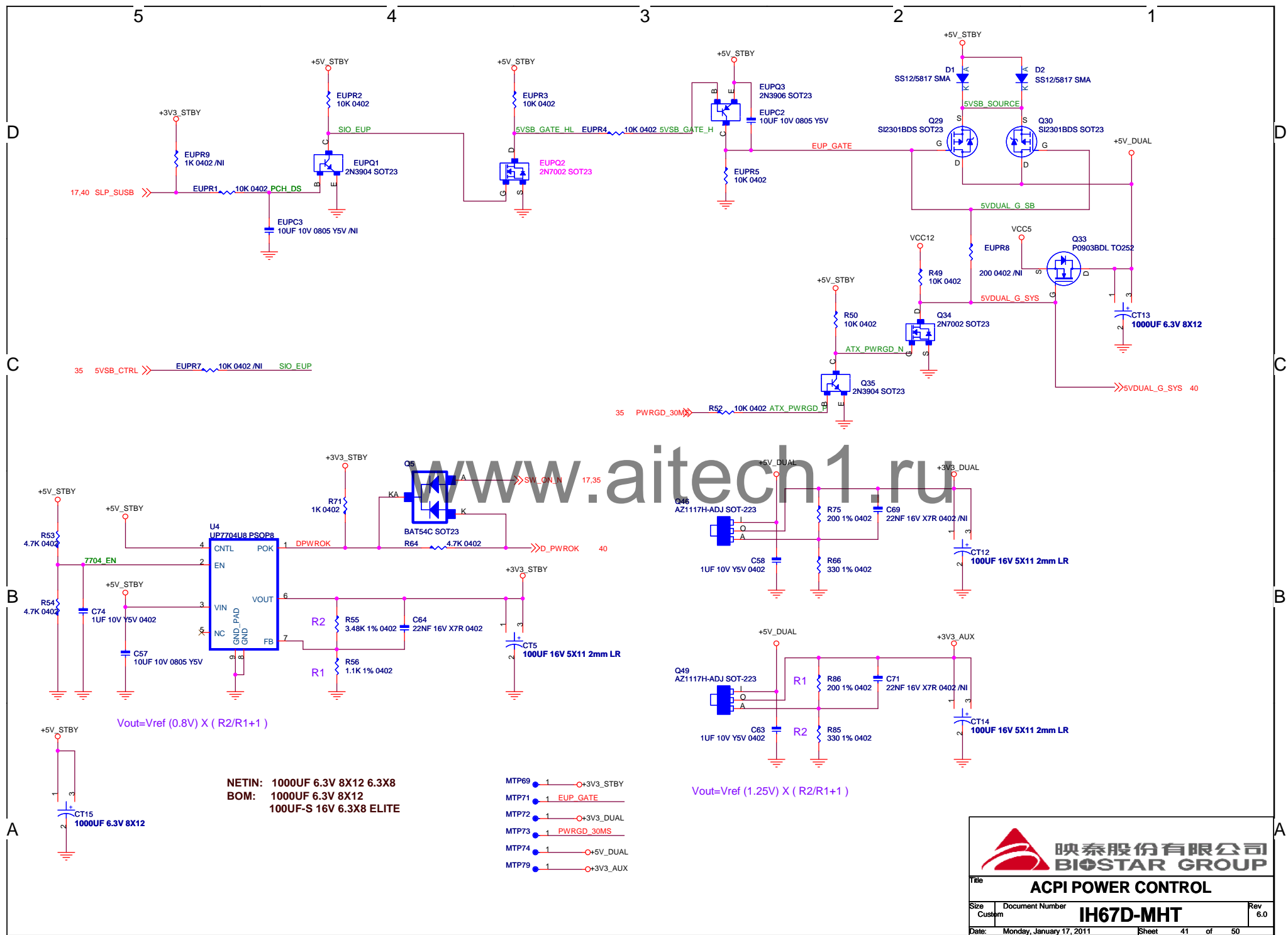
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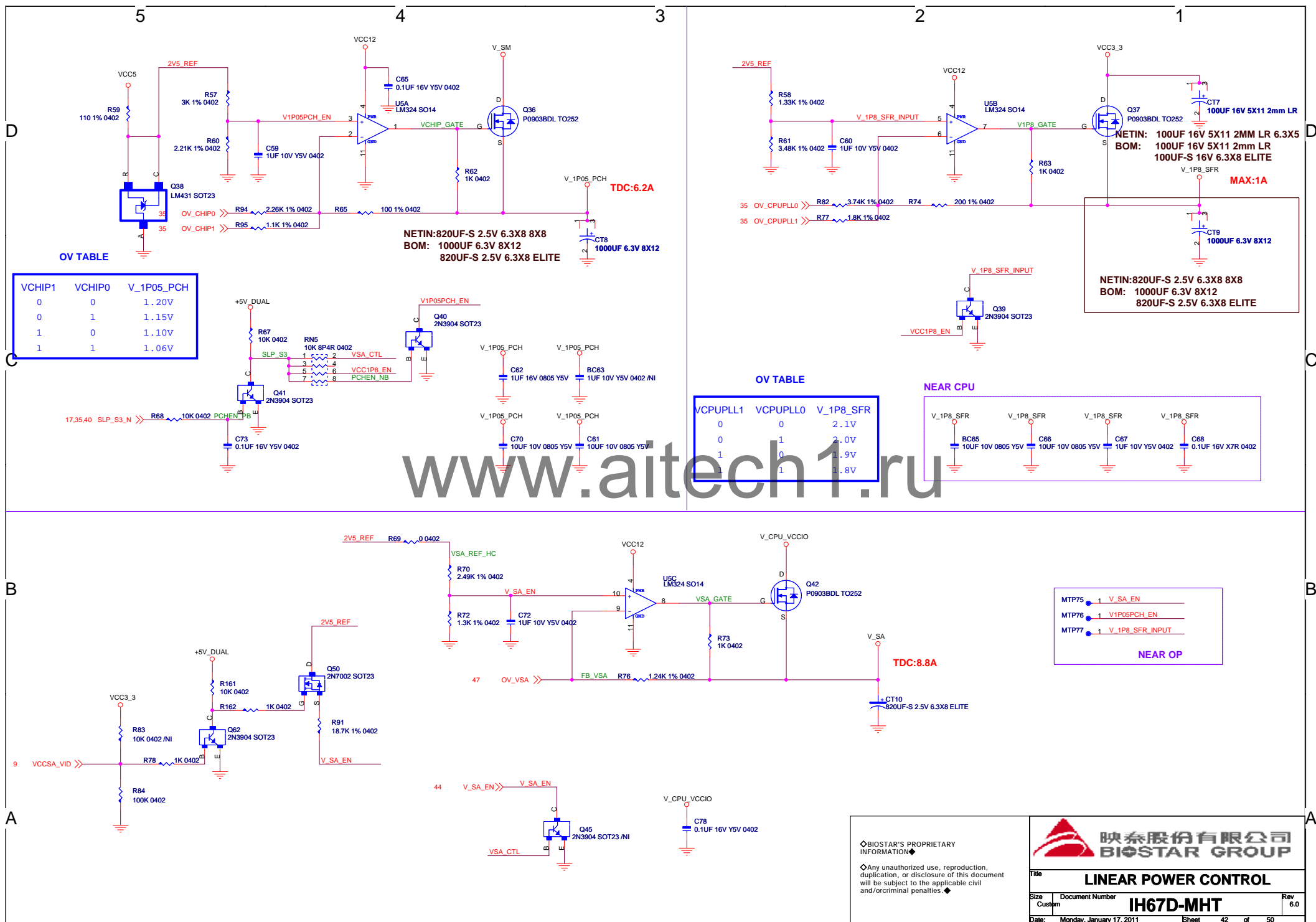
Size	Document Number
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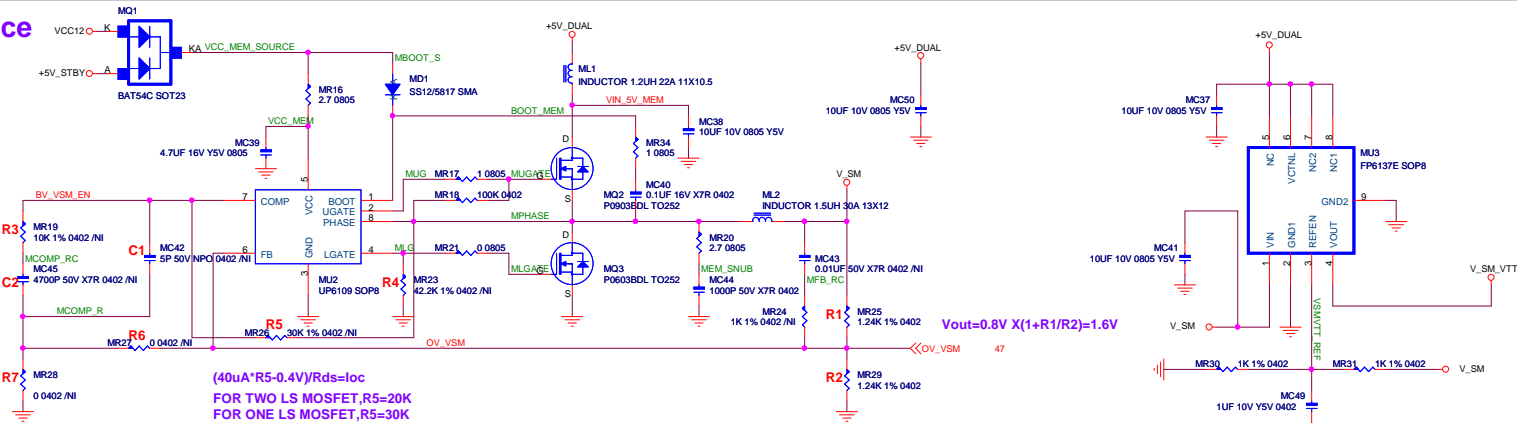




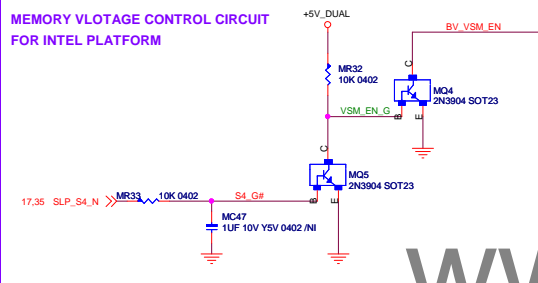


# MEMORY PART:M+Reference

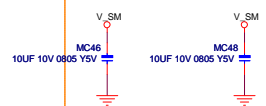
	FP6321A	UP6101B	FP6327
R3	NI	13.7K 1% 0402	
R4	NI	26.1K 1% 0402	
R5	20K 0402	NI	
R6	NI	0 0402	
R7	NI	NI	
C1	NI	5P 50V NPO 0402	
C2	NI	4700P 50V X7R 0402	



## MEMORY VLOTAGE CONTROL CIRCUIT FOR INTEL PLATFORM



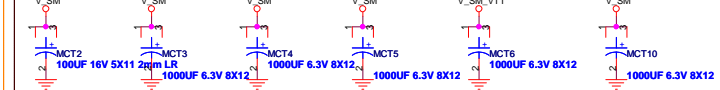
## Between CPU and DIMM



## NETIN:820UF-S 2.5V 6.3X8 8X8

BOM: 1000UF 6.3V 8X12

820UF-S 2.5V 6.3X8 ELITE



NETIN: 100UF 16V 5X11 2MM LR 6.3X5

BOM: 100UF 16V 5X11 2mm LR

100UF-S 16V 6.3X8 ELITE

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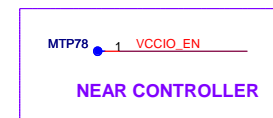
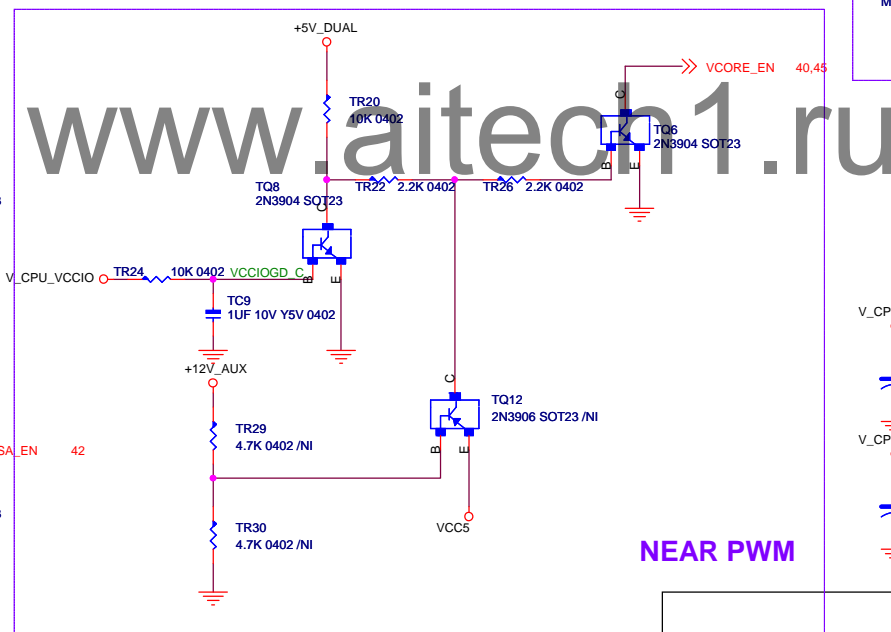
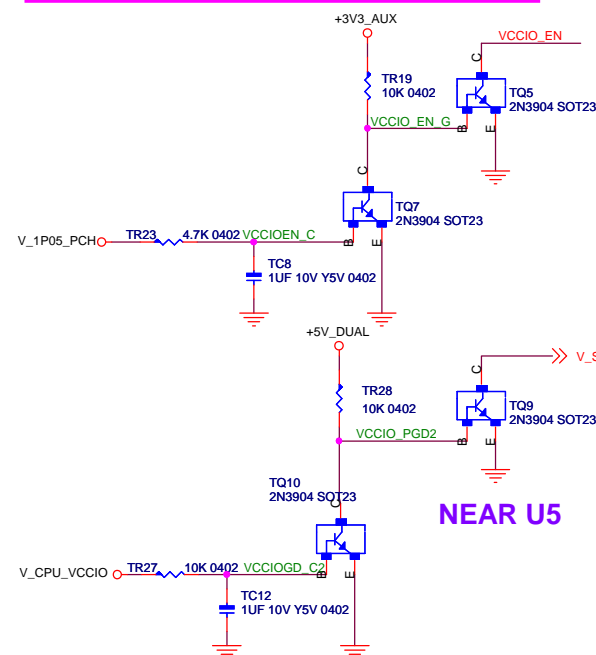
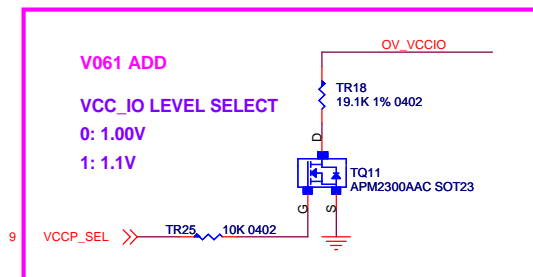
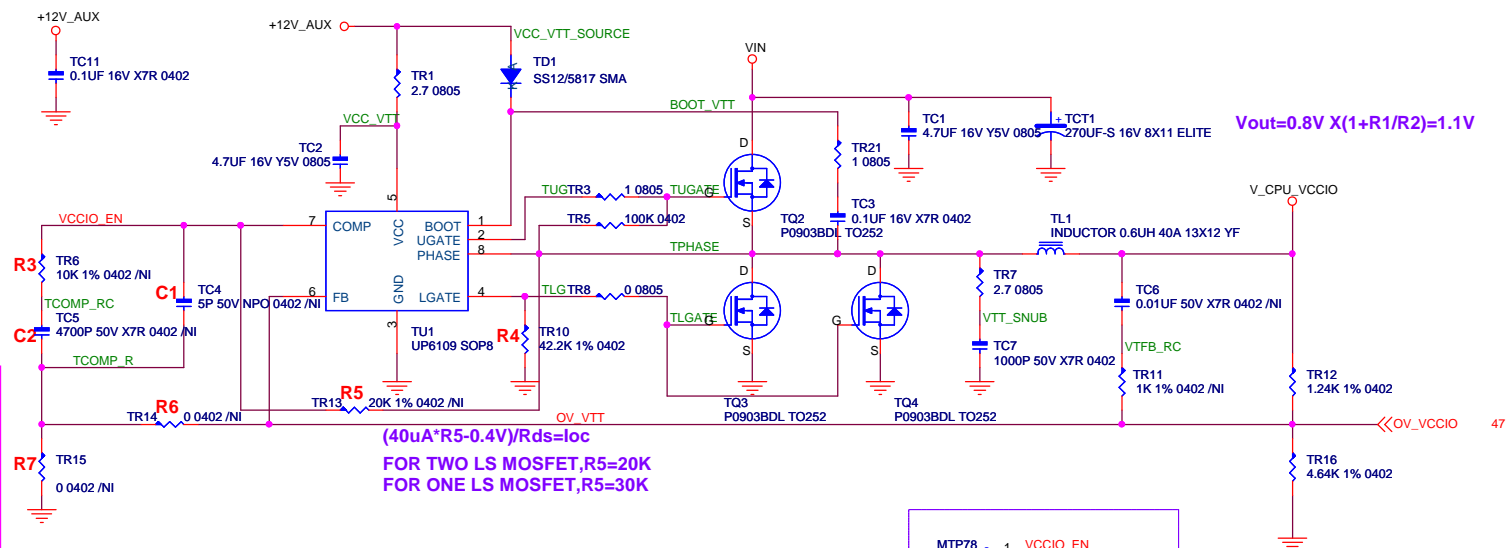
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<b>VSM DC-DC Conver</b> <b>IH67D-MHT</b>	
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# VTT POWER PART:T+Reference

	FP6321A	UP6101B	FP6327
R3	NI	13.7K 1% 0402	
R4	NI	26.1K 1% 0402	
R5	20K 0402	NI	
R6	NI	0 0402	
R7	NI	NI	
C1	NI	5P 50V NPO 0402	
C2	NI	4700P 50V X7R 0402	



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# CPU POWER PART:P+Reference

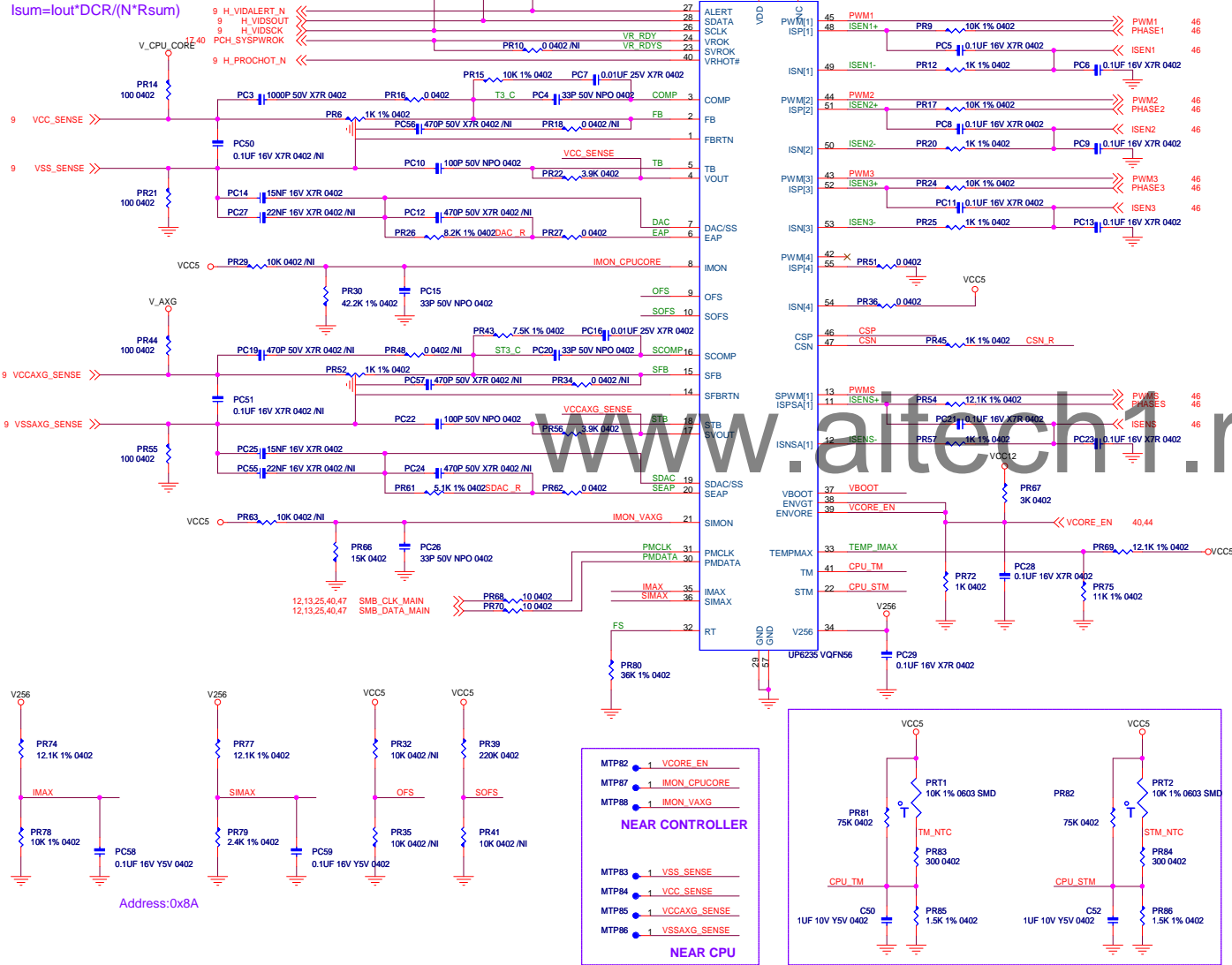
# VRD12: 3+1 HIGH1+LOW2

D/源供 CHOKE 0.6uH/40A/  
DCR0.8m/ELDA-1312-R60M-P/磁感..

$L/DCR=R_{csp} \cdot C_{cs}$   
 $N \cdot L/DCR=R_{sw} \cdot C_{sum}$

$R_{ll}=DCR \cdot R_{droop}/R_{csn}/N$   
 $=0.8m\Omega \cdot 6.8K\Omega / 1K\Omega / 3$   
 $=1.7m\Omega$

$I_{sum}=I_{out} \cdot DCR/(N \cdot R_{sum})$



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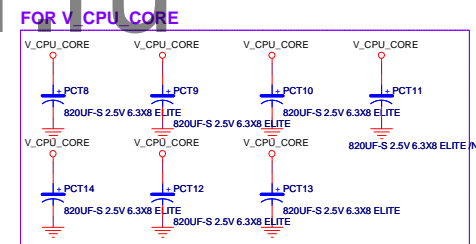
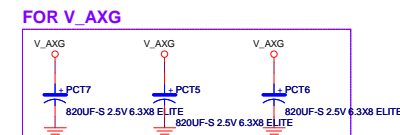
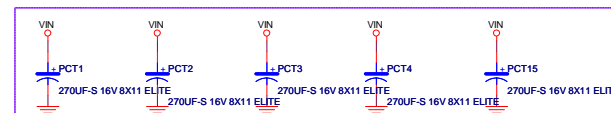
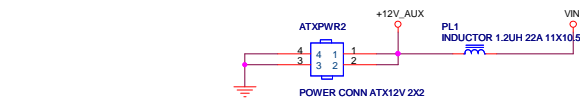
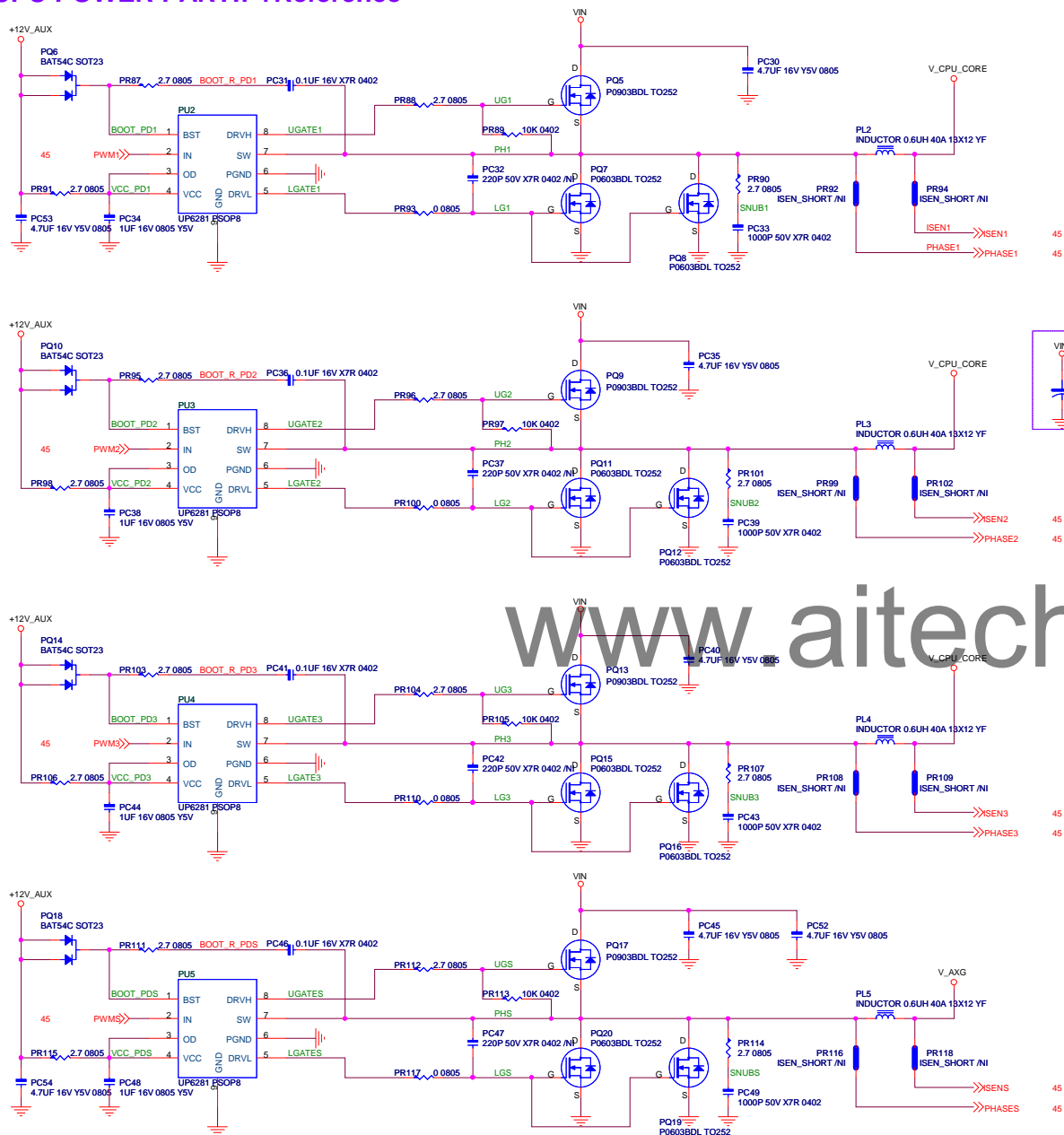
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**BIOSSTAR GROUP**

File: **VCORE VREG1**

Size: Custom Document Number: **IH67D-MHT** Rev: 6.0

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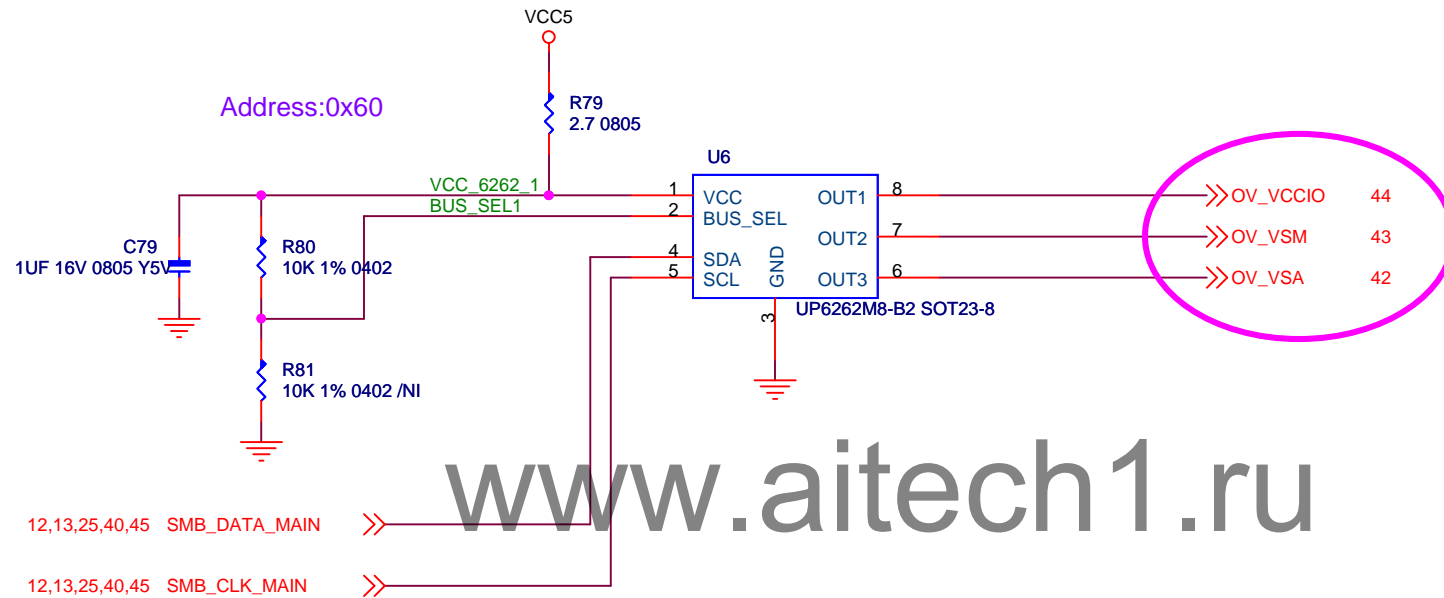
# CPU POWER PART:P+Reference



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VCORE VREG2		
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Title **OVER VOLTAGE**

Size A Document Number **IH67D-MHT**

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5

4

3

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1

D

C

B

A

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Title			RESERVED FOR AMT POWER
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5

4



3

2

1

NETIN: 100UF 16V 5X11 2MM LR 6.3X5  
BOM: 100UF 16V 5X11 2mm LR  
100UF-S 16V 6.3X8 ELITE

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	Size Custom	Document Number <b>IH67D-MHT</b>	Rev 6.0
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